

Receiving SONY DmCn Remote Format

Using Remote Control Timer for Detecting SONY Remote Format

DESCRIPTION

This application note presents a suite of software routines which may be incorporated into a user's application to allow HMS81C2232/48, HMS81C2332/48 series micro-controllers build-in Remote Control Timer.

The software supports all members of the HMS800 series build-in capture mode, and may easily be modified for compatibility with any of the HMS800 compatible micro-controllers.

REMOTE CONTROL TIMER CONFIGURATION

Description of Remote control Timer.

The 8-bit remote control timer has a pulse width measurement function with a resolution of 8 bits. Pulse width is measured from a difference in count value when the valid edge has been detected while the timer operates in the free-running mode.

Registers Controlling 8-Bit Remote Control Timer.

The following three types of registers control the 8-bit remote control timer.

- Remote control timer control register (RTCR)
- Remote control timer capture registers (RTCP0 and RTCP1)
- 8-bit timer register (RT)

(1) Remote control timer control register(RTCR)

This register enables or disables the operation of the 8-bit timer (RT), and sets the count clock. TMC9 is set by using a 1-bit or 8-bit memory manipulation instruction. This register is initialized to 00_H by RESET input.

(2) Remote control timer capture registers (RTCP0 and RTCP1)

These 8-bit registers capture the contents of the 8-bit timer

(RT). The capture operation is performed in synchronization with the valid edge input to the TI pin (capture trigger). The contents of RTCP0 are retained until the next rising edge of the TI pin is detected. The contents of RTCP1 are retained until the next falling edge of the TI pin is detected.

RTCP0 and RTCP1 can be read by using an 8-bit memory manipulation instruction. The values of these registers are initialized to 00_H by RESET input.

(3) 8-bit timer register (TM9)

This 8-bit register counts the count pulse. It can be read by using an 8-bit memory manipulation instruction. The value of this register is initialized to 00_H by RESET input or by clearing the RTST bit.

Operation of 8-Bit Remote Control Timer.

The 8-bit remote control timer operates as a pulse width measuring circuit. The width of a high-level or low-level external pulse input to the TI pin is measured by operating the 8-bit timer (TM9) in the free-running mode. Detection of the valid edge is sampled every 2 cycles of the count clock selected by TCL0, TCL1 and TCL2, and the capture operation is not performed until the valid level has been detected two times.

Therefore, the pulse width input to the TI pin must be 5 or more of the count clock set by TCL0, TCL1 and TCL2, regardless of whether the level is high or low. If the pulse width is less than 5 clocks, it cannot be detected, and the capture operation is not performed. The value of timer register 9 (TM9) is loaded to and retained in the capture registers (CP90 and CP91) in synchronization with the valid edge of the pulse input to the TI pin, as shown in Figure 0-1. Figure 0-2 shows the timing of pulse width measurement.

The Remote Timer control register is shown in Figure 1.

The RTCP0, RTDR and RT are in same address. In the capture mode, reading operation is read the RTCP0, not RT because path is opened to the RTCP0, and RTDR is only for writing operation.

	R/W	R/W	R/W	R/W	R/W	R/W		
	5	4	3	2	1	0		
RTCR	-	-	RCAP	RTCK2	RTCK1	RTCK0	RTCN	RTST

ADDRESS: 0E7_H
INITIAL VALUE: --00 0000_B

Bit Name	Bit Position	Description
RCAP	RTCR.5	0: Timer/Counter mode 1: Capture mode selection flag
RTCK2	RTCR.4	000: 8-bit Timer, Clock source is $f_{XIN} \div 8$
RTCK1	RTCR.3	001: 8-bit Timer, Clock source is $f_{XIN} \div 32$
RTCK0	RTCR.2	010: 8-bit Timer, Clock source is $f_{XIN} \div 128$ 011: 8-bit Timer, Clock source is $f_{XIN} \div 256$ 100: 8-bit Timer, Clock source is $f_{XIN} \div 512$ 101: 8-bit Timer, Clock source is $f_{XIN} \div 1024$ 110: 8-bit Timer, Clock source is $f_{XIN} \div 2048$ 111: 8-bit Timer, Clock source is $f_{XIN} \div 4096$
RTCN	RTCR.1	0: Timer count pause 1: Timer count start
RTST	RTCR.0	0: When cleared, stop the counting. 1: When set, Timer 0 Count Register is cleared and start again.

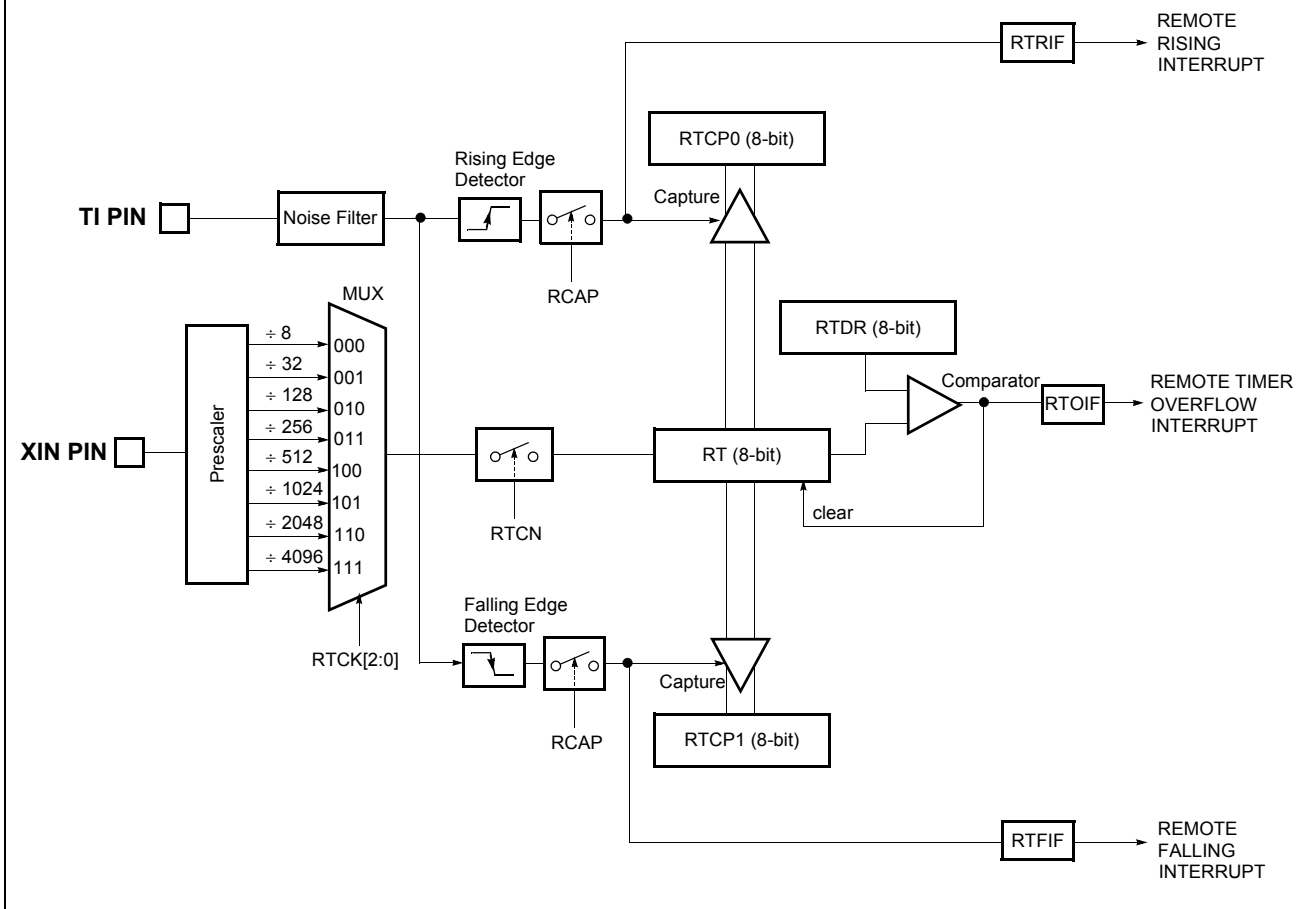


Figure 1. RTCR Register & Block Diagram of Remote Control Timer

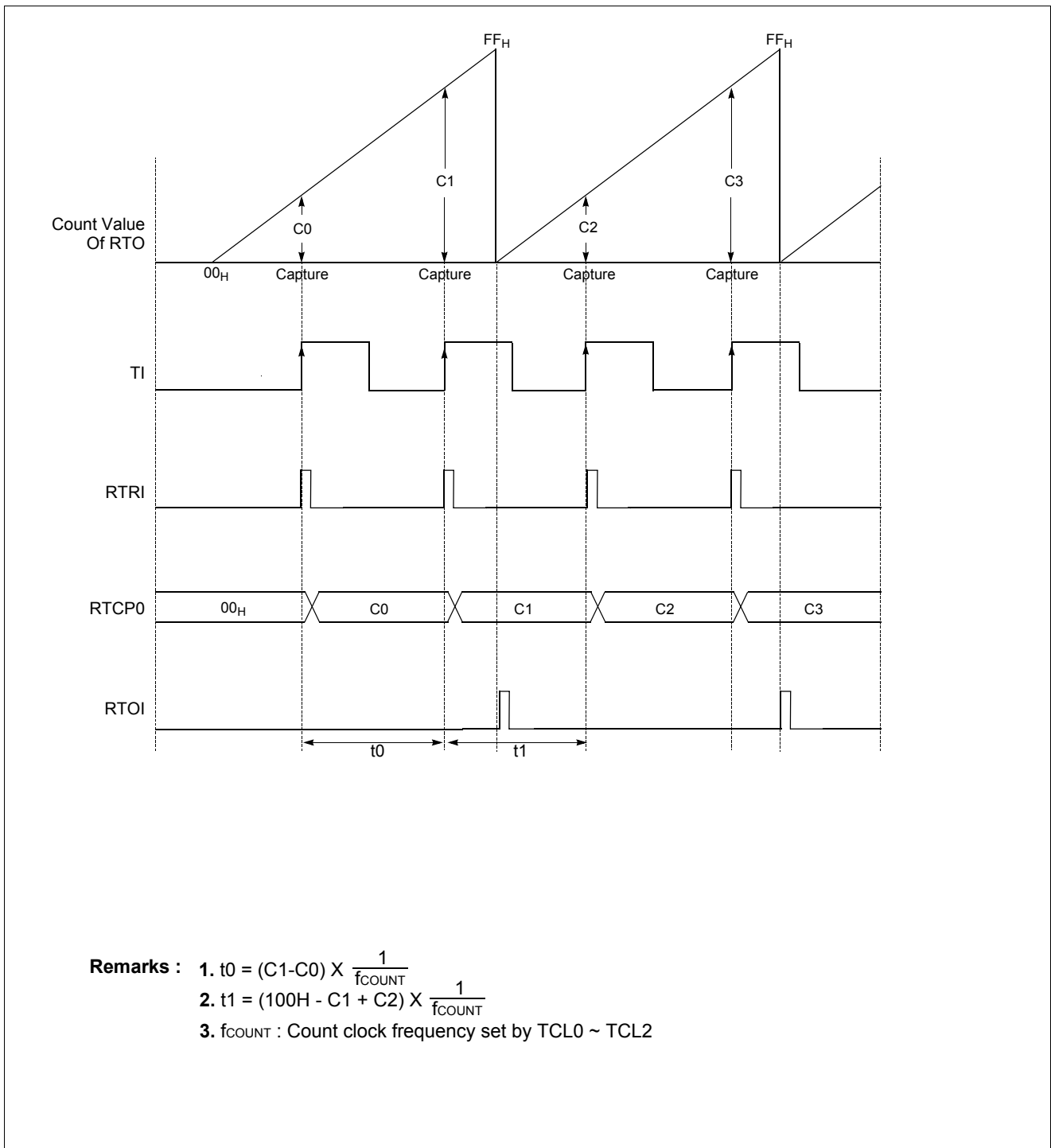


Figure 0-1 To measure pulse width in synchronization with rising edge

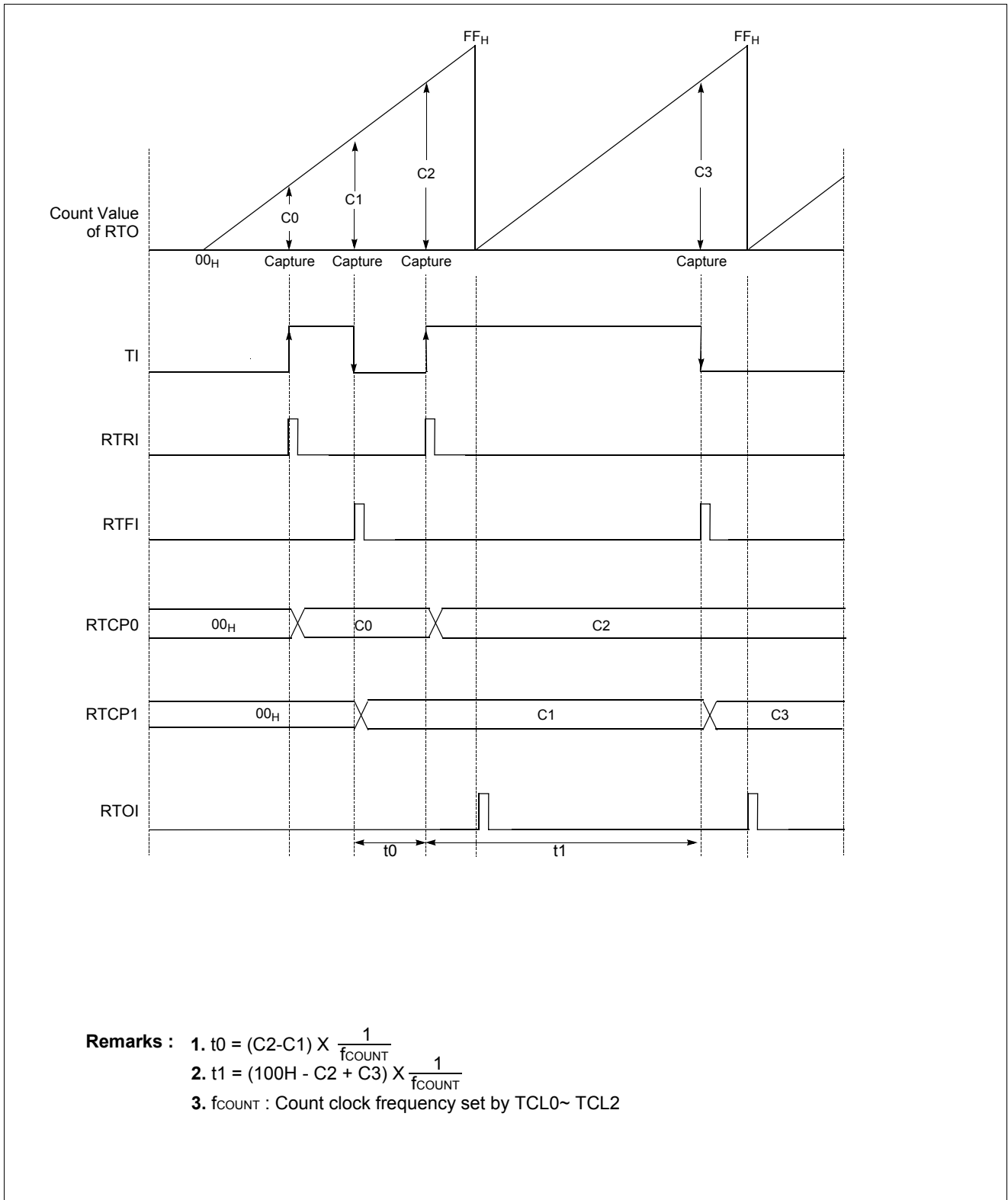


Figure 0-2 To measure pulse width in synchronization with both rising and falling edge

THE HARDWARD CONNECTION

A typical hardware connection is illustrated in Figure 2. The HMS800 series makes interface with IR receiver through TI port. In most systems, the interface is con-

nected to circuitry like IR receiver parts that receive remote signals with carrier frequency. The initial state of remote signal input is “High” level condition.

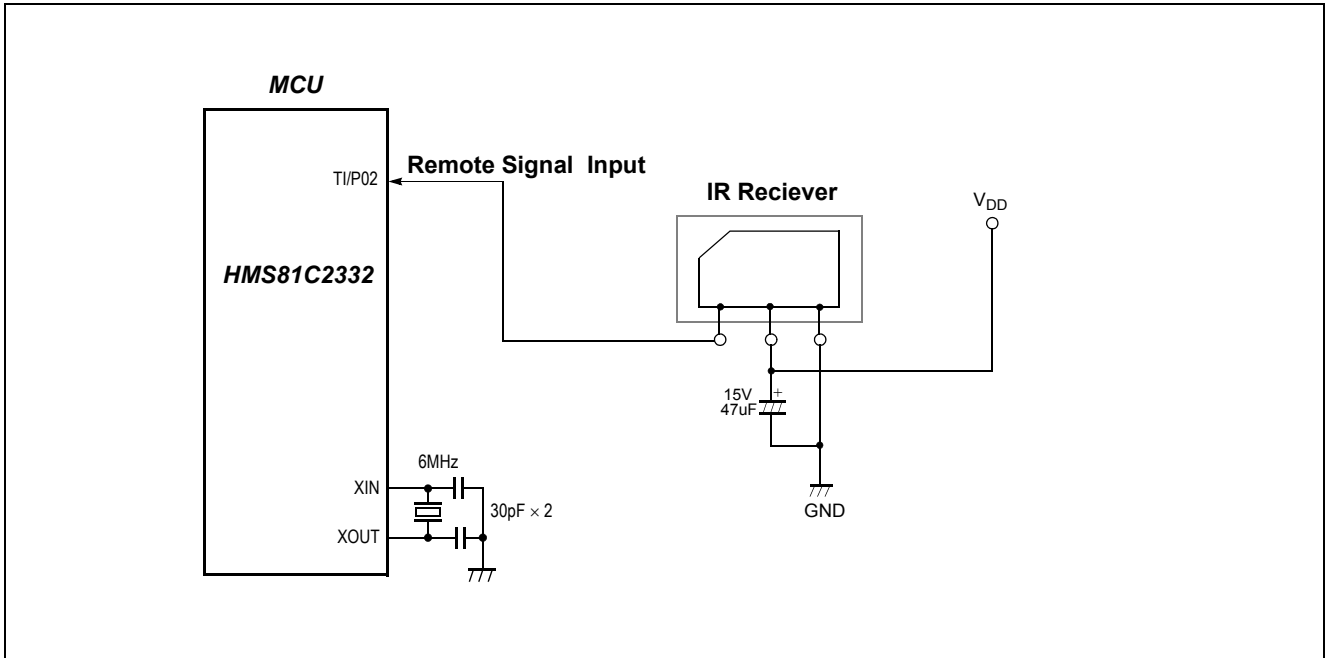


Figure 2. Hardware Connection

SONY-DmCn FORMAT

A typical SONY-DmCn remote signal format is shown in Figure 3.

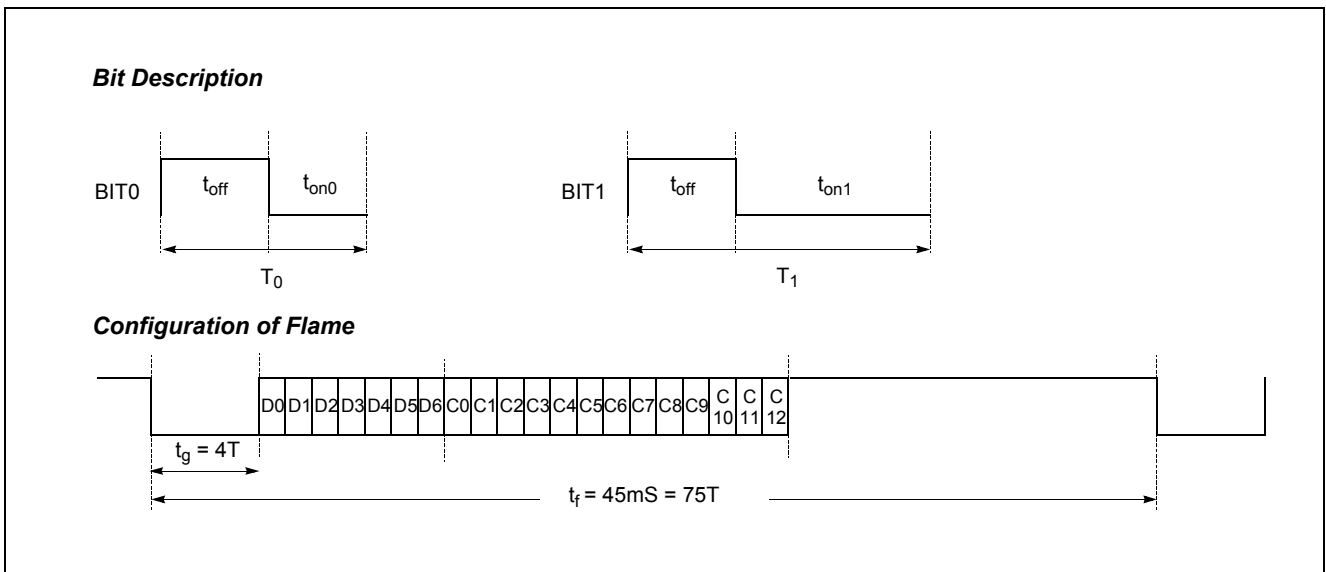


Figure 3. SONY-D7C13 Format

Guide pulse and bit format.

The guide pulse and bit format of the remote control signals shall be as follows:

Items	Symbol	Time	Tolerance
Duration of guide pulse	t_g	2.4mS	$\pm 0.015mS$
Data bit OFF time	t_{off}	0.6mS	$\pm 0.015mS$
Data bit ON time	"1"	t_{on1}	$\pm 0.015mS$
	"0"	t_{on0}	$\pm 0.015mS$
Period of data bit	"1"	T_1	$\pm 0.03mS$
	"0"	T_0	$\pm 0.03mS$
Frame period	t_f	45.0mS	$\pm 1.2mS$
Sub-carrier frequency		40kHz	-

In the receiver, a tolerance of $\pm 1\%$ is added to each of the tolerances above with the aging of equipment and the variation of a ceramic resonator being considered.

Code Format

The code formats employed are a 20-bit configurations as shown below.

(1) Guide Pulse.

Guide pulse is the discrimination signal that is prefixed to

determine the start of the serial remote control signal composed.

(2) Category Code.

This code is assigned to each product category subjected to the remote control system and consists of 13 bits.

(3) Data Code

This code consists of 7 bits to control the necessary control functions for the specified product category.

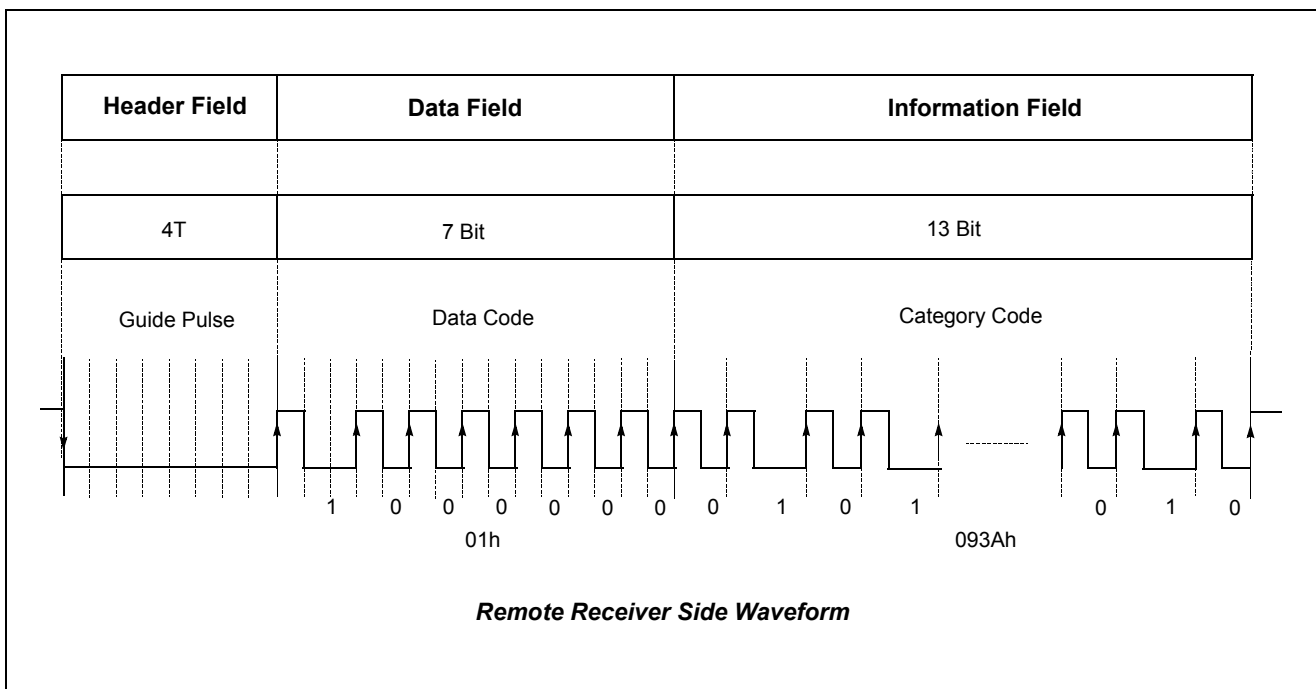


Figure 4. Format of SONY-D7C13 for Number-2 Key at DVDP

Number of frames transferred

(1) Single transmission.

Three frames.

Proper functions are thereby assured even when external disturbance occurs.

(2) Continuous transmission. Output transmission continues while data is entered successively and nor-

mally from the keyboard. When the end of data input by a key is detected, the output transmission will end at the end of the current output frame.

Cancel Time

The examples of continuous/non-continuous key pressing processes (Frame cancel time is set at the standard duration, 100mS)

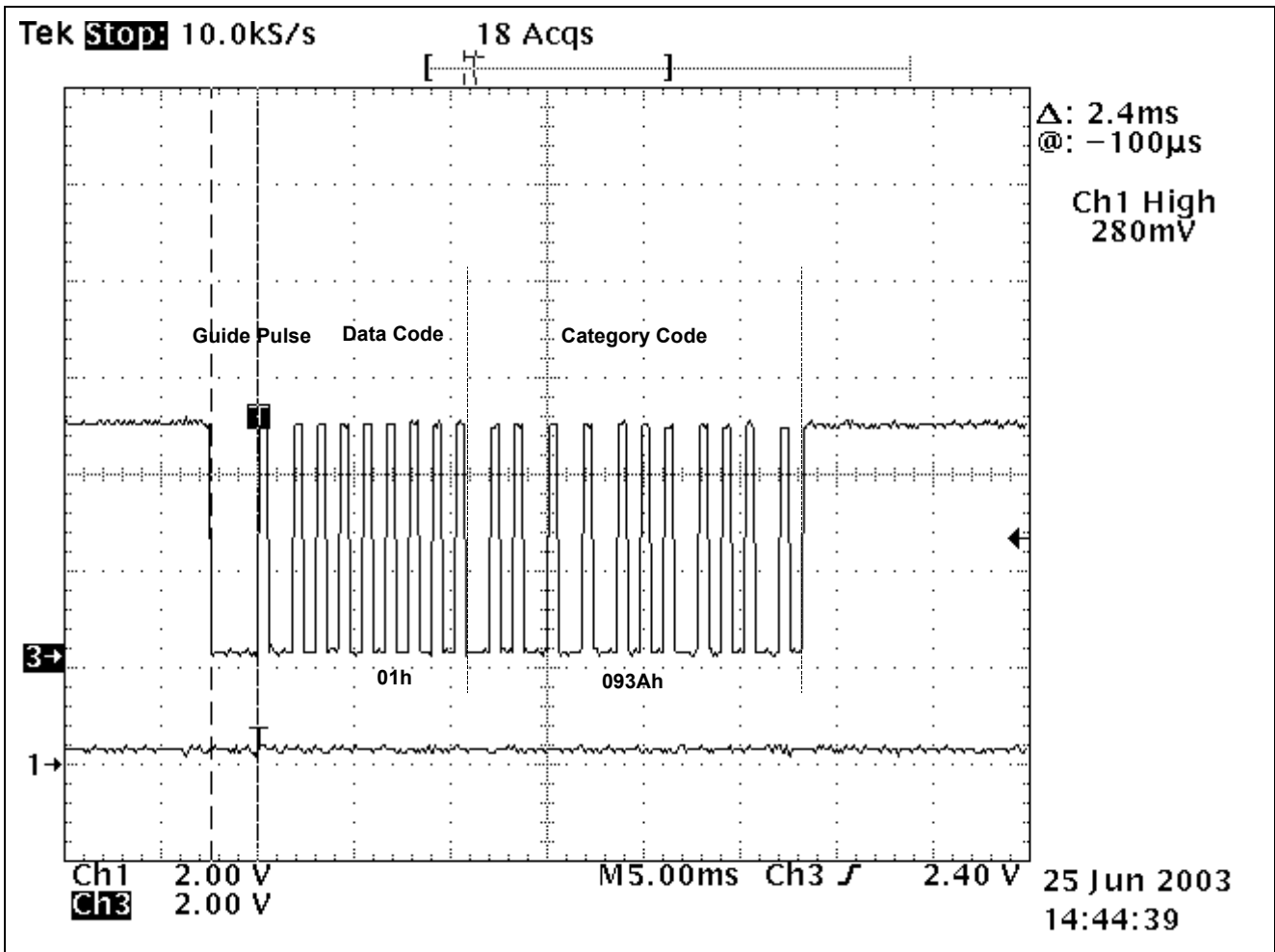


Figure 5. Waveform of SONY-D7C13 for Number-2 Key at DVDP

Design of reception Circuit

Relationship with the operation of the equipment.

Care should be taken to prevent the occurrence of any faulty operations, no-operations, etc. to the equipment even when meaningless signals (noise, another category signal, etc.) are input to the SIRCS signal input terminals

(infrared and wired).

Design requirements of reception circuit.

1) Clock deviation.

The clock deviation between transmission and reception is $\pm 2\%$ or less.

2) Bit format check.

The tolerances are given to each bit, including the guide pulse. Then, t_{off} and t_{on} must be read separately, and the bit format must be checked. However, when the checking way is to be simplified, t_{off} in the first place and then $t_{off} + t_{on}$ may be read.

3) Number of bits check.

20-bit format is regarded as valid only when the data signal consist of 20 bits is received. A data signal is invalid when the data signal consists of 19 bits or less, or 21 bits or more. (When a data signal consist of 21 bits or more comes in, 20 bits out of the 21 bits or more must not be read as the data to be dealt as a valid command.)

4) A signal period(45mS).

A signal period shall also be detected (The frame shall be detected.)

THE SOFTWARE STRUCTURE

An example software algorithm is listed in Source Program. The function of example source of HMS81C2332 store 3-bytes remote data buffer with SONY-D7C13 format data.

A) Remote falling interrupt service routine.

1. Check the remote state buffer (REM_JMP) to find out whether first falling interrupt is occurred.
2. If first falling interrupt occurred, increase the remote state buffer (REM_JMP). And then exit remote falling interrupt service routine.
3. If not first falling interrupt, exit remote falling interrupt service routine without any operation.

B) Remote rising interrupt service routine.

1. Check the remote state buffer (REM_JMP) to find out whether the state is header field or data & information field.
2. If header field, check pulse width whether it is $2.4mS \pm 0.015mS$. if it was true, increase the remote state buffer (REM_JMP). And then exit remote falling interrupt service routine.
3. If data & information field, check the pulse width whether data bit is "1" or "0". And then shifted bit data 20 times (data field = 7 bits and information field = 13 bits).
4. If shifted 20 times, store rREM_Data rCustom1, rCustom1 with data field & information field. And then initialize REM_JMP and exit remote falling interrupt service routine.

C) Remote timer interrupt service routine.

1. Check the SONY-D7C13 frame period (about 45mS) to find out whether the state is initial.
2. If greater than SONY-D7C13 frame period, initialize all remote buffer RAMs.
3. If less than SONY-D7C13 frame period, exit remote timer interrupt service routine without any operation.

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1. Source Program

GMS800 series MICOM ASSEMBLER Thu May 06 14:00:59 2004
(PAGE 1)

```

1          page      10000
2          ;*****;
3          ;                      Using Remote Timer                      ;
4          ;*****;
5          ;
6          ;                      MICOM : HMS81C2348 (ROM:48K,64SDIP)      ;
7          ;                      X-tal : 6MHz - 0.33334uS 1cycle          ;
8          ;                      0.666uS 2cycle                          ;
9          ;                      1uS 3cycle                               ;
10         ;
11         ;=====;
12         ; PROGRAMMER : Kyung Sang Yun                2002/12/01  VER1.0 ;
13         ;=====;
14         ;                      HMS81C2348                                ;
15         ;                      -----                                ;
16         ;                      0 Not Used |1 FIP07 FIP08 64| Not Used 0 ;
17         ;                      0 Not Used |2 FIP06 FIP09 63| Not Used 0 ;
18         ;                      0 Not Used |3 FIP05 FIP10 62| Not Used 0 ;
19         ;                      0 Not Used |4 FIP04 FIP11 61| Not Used 0 ;
20         ;                      0 Not Used |5 FIP03 FIP12 60| Not Used 0 ;
21         ;                      0 Not Used |6 FIP02 FIP13 59| Not Used 0 ;
22         ;                      0 Not Used |7 FIP01 FIP14 58| Not Used 0 ;
23         ;                      0 Not Used |8 FIP00 FIP15 57| Not Used 0 ;
24         ;                      I +5V |9 VDD1 VDISP 56| Not Used 0 ;
25         ;                      0 0V |10 VSS1 VDD2 55| Not Used 0 ;
26         ;                      0 Xin |11 XIN FIP16 54| Not Used 0 ;
27         ;                      0 Xout |12 XOUT FIP17 53| Not Used 0 ;
28         ;                      I Not Used |13 P07 FIP18 52| Not Used 0 ;
29         ;                      I Reset |14 /RESET FIP24 51| Not Used 0 ;
30         ;                      0 Not Used |15 SCK1 FIP25 50| Not Used 0 ;
31         ;                      I Not Used |16 SI1 FIP26 49| Not Used 0 ;
32         ;                      0 Not Used |17 SO1 FIP27 48| Not Used 0 ;
33         ;                      0 Not Used |18 P24 FIP28 47| Not Used 0 ;
34         ;                      I Not Used |19 P00 FIP29 46| Not Used 0 ;
35         ;                      0 Not Used |20 P01 FIP30 45| Not Used 0 ;
36         ;                      0 Remote IN |21 P02 FIP31 44| Not Used 0 ;
37         ;                      0 Not Used |22 AVSS FIP32 43| Not Used 0 ;
38         ;                      0 Not Used |23 P03 FIP33 42| Not Used 0 ;
39         ;                      0 Not Used |24 P04 FIP34 41| Not Used 0 ;
40         ;                      0 Not Used |25 P05 FIP35 40| Not Used 0 ;
41         ;                      0 Not Used |26 P06 FIP36 39| Not Used 0 ;
42         ;                      I 0V |27 VSS0 P50 38| Not Used 0 ;
43         ;                      0 Not Used |28 AVDD P51 37| Not Used 0 ;
44         ;                      I +5V |29 VDD0 P52 36| Not Used 0 ;
45         ;                      0 Not Used |30 P64 P53 35| Not Used 0 ;
46         ;                      0 Not Used |31 P63 P54 34| Not Used 0 ;
47         ;                      0 Not Used |32 P62 P55 33| Not Used 0 ;
48         ;                      -----                                ;
49         ;
50         ;=====;
51         ;
52         ;=====;
53
54         ;*****;
55         ;                      HMS81C2248 I/O PORT & FUNCTION REGISTER Address DEFINE ;
56         ;*****;
57         ;

```

```

58      P0      EQU      0C0H      ;Port0 register
59      P0IO    EQU      0C1H      ;Port0 data I/O direction register
60      P1      EQU      0C2H      ;Port1 register
61      P2      EQU      0C4H      ;Port2 register
62      P2IO    EQU      0C5H      ;Port2 data I/O direction register
63      P3      EQU      0C6H      ;Port3 register
64      P4      EQU      0C8H      ;Port4 register
65      P5      EQU      0CAH      ;Port5 register
66      P6      EQU      0CCH      ;Port6 Register
67      ;
68      RPR      EQU      0DFH      ;RAM Page Selection Register
69
70      IENH     EQU      0E2H      ;Interrupt Enable Register High
71      IENL     EQU      0E3H      ;Interrupt Enable Register Low
72
73      IRQH     EQU      0E4H      ;Interrupt Request Flag Register High
74      IRQL     EQU      0E5H      ;Interrupt Request Flag Register Low
75
76      IEDS     EQU      0E6H      ;External Interrupt Edge Selection Register
77
78      RTCR     EQU      0E7H      ;Remote Timer Control Register
79
80      RTDR     EQU      0E8H      ;Remote Timer Data Register
81      RTCPO    EQU      0E8H      ;Remote Timer Capture Register0
82      ;
83      BITR     EQU      0ECh      ;Basic Interval Timer Register (Read)
84      CKCTLR   EQU      0ECh      ;                               (Write)
85      ;
86      WDTR     EQU      0EDh      ;Watch Dog Timer Register
87      PFDR     EQU      0EFh      ;PDF Control Register
88      ;
89      PSR      EQU      0F4h      ;Port Select Register
90
91      ;*****;
92      ;                               RAM Allocation                               ;
93      ;*****;
94
95      rCustom_1 DS      1          ;Remocon Custom1 Data
96      rCustom_2 DS      1          ;Remocon Custom2 Data
97      rREM_Data DS      1          ;Remocon Data
98
99      rRemoconCNT DS      1          ;Remocon Frame Max. Timer
100
101      rREM_JMP DS      1
102      rData_CAP DS      1
103
104      rSony_BUF DS      3
105      rSony_BUF1 EQU      rSony_BUF+1
106      rSony_BUF2 EQU      rSony_BUF+2
107
108      ;*****;
109      ;                               Constant Definition                               ;
110      ;*****;
111
112      ; ***** Control Port Name Assignment *****
113
114      ;
115      ;***** Port0 *****
116
117      pRemocon EQU      2,P0      ;Remocon Input
118
119      ;*****;

```

```

120          ;                      MACRO Definition                      ;
121          ;*****;
122
123          SAVE      MACRO                      ;Register Save
124
125                      PUSH      A
126                      PUSH      X
127                      PUSH      Y
128
129                      ENDM
130
131          RESTORE   MACRO                      ;Register Restore
132
133                      POP       Y
134                      POP       X
135                      POP       A
136
137                      ENDM
138
139          INCR      MACRO
140
141                      INC       \1           ;\1<--RAM Name
142                      LDA       \1           ;\2<--Compare Num.
143                      CMP       \2           ;\3<--Branch Label
144                      BNE       \3
145                      LDM       \1,#0
146
147                      ENDM
148
149          ;*****;
150          ;                      Interrupt Vector Table                    ;
151          ;*****;
152
153          ORG       0FFE0H
154 FFE0 5181        DW       Not_Used           ; Basic Interval Timer
155 FFE2 5181        DW       Not_Used           ; Watch Dog Timer
156 FFE4 5181        DW       Not_Used           ; A/D Converter
157 FFE6 5181        DW       Not_Used           ; Not Used
158 FFE8 5181        DW       Not_Used           ; Not Used
159 FFEA 5181        DW       Not_Used           ; Timer1
160 FFEC 5181        DW       Not_Used           ; Timer0
161 FFEE 5181        DW       Not_Used           ; SIO3
162 FFF0 5181        DW       Not_Used           ; SIO1
163 FFF2 5181        DW       Not_Used           ; Key Scan Interrupt
164 FFF4 2B81        DW       RTimer_ISP       ; Remote Timer(Overflow)
165 FFF6 8280        DW       Falling_ISP      ; Remote Falling Edge Capture
166 FFF8 9A80        DW       Rising_ISP      ; Remote Rising Edge Capture
167 FFFA 5181        DW       Not_Used           ; Ext.INT1
168 FFFC 5181        DW       Not_Used           ; Ext.INT0
169 FFFE 0080        DW       Reset            ; Reset
170
171          ;*****;
172          ;                      Program Initial Part                    ;
173          ;*****;
174
175          ORG       08000h                   ;HMS81C2232/2332 Program Start Address
176 Reset:
177 8000 60          DI                          ;Disable All Interrupt
178
179          ;=====;
180          ;  RAM Clear Routine  ;
181          ;=====;

```

```

182
183 8001 1E00          LDX    #0
184 8003 3E00          LDY    #0          ;
185
186 8005 C400          LDA    #0          ;Page0 RAM Clear(0000h ~ 00BFh)
187 8007 FB           STA    {X}+
188 8008 5EC0          CMPX   #0C0h
189 800A 70F9          BNE    RAM_Clear0
190
191 800C 9E           INC    Y
192 800D F8DF00        STY    !RPR          ;!Page Select
193 8010 C0           SETG
194
195 8011 1E00          LDX    #0
196
197 8013 C400          LDA    #0          ;
198 8015 FB           STA    {X}+
199 8016 5E00          CMPX   #00h
200 8018 70F9          BNE    RAM_Clear1
201
202 801A 9E           INC    Y
203 801B 7E05          CMPY   #5          ;Page1~Page4 RAM Clear(0100h ~ 03FFh)
204 801D D006          BCS    RAM_Clear_Bye
205
206 801F F8DF00        STY    !RPR
207 8022 C0           SETG          ;
208
209 8023 2FEE          BRA    RAM_Clear1
210
211
212 8025 40           CLRG          ;Page0 Select
213
214 8026 1EFF          LDX    #0FFh       ;Initial Stack Pointer
215 8028 8E           TXSP          ;
216
217 8029 E400EF        LDM    PFDR,#00    ;Power Fail Detect Freeze Mode...
218
219
220 802C 3B3E80        CALL   Initial_IO  ;I/O Port Initial
221 802F 3B6380        CALL   Initial_Reg ;Register Initial
222 8032 3B7980        CALL   Initial_RAM ;RAM Initial
223
224 8035 E0           EI           ;Enable Interrupt
225
226 ;*****;
227 ;           Main Program Part           ;
228 ;*****;
229
230 Main:
231 8036 3B5C80        CALL   IO_Direction ;I/O Direcction Refresh
232
233
234 8039 FF           NOP
235 803A FF           NOP
236 803B FF           NOP
237
238
239 803C 2FF8          BRA    Main          ;Main End
240
241
242 ;*****;
243 ;           Program Initial Part Sub-Routines           ;

```

```

244 ;*****;
245
246 ;=====;
247 ; Initial I/O PORT ;
248 ;=====;
249 Initial_IO:
250 803E E4FBC1 LDM P0IO,#1111_1011b ;
251 8041 E400C0 LDM P0,#0000_0000b ;P02 Remocon Input (Input)
252
253 8044 E4FFC5 LDM P2IO,#1111_1111b ;
254 8047 E400C4 LDM P2,#0000_0000b
255
256 804A E400C6 LDM P3,#0000_0000b ;
257
258 804D E400C8 LDM P4,#0000_0000b ;
259
260 8050 E400CA LDM P5,#0000_0000b ;
261
262 8053 E400CC LDM P6,#0000_0000b ;
263
264 8056 E400E6 LDM IEDS,#0000_0000b ;
265 8059 E400F4 LDM PSR,#0000_0000b ;
266
267
268 IO_Direction:
269 805C E4FBC1 LDM P0IO,#1111_1011b ;
270 805F E4FFC5 LDM P2IO,#1111_1111b ;
271
272 8062 6F RET
273
274 ;=====;
275 ; Initialize control register ;
276 ;=====;
277 Initial_Reg:
278 8063 E4FFE8 LDM RTDR,#0FFh ;RTimer Input Capture Max Initial Value 32,768uS
279 8066 E42BE7 LDM RTCR,#0010_1011b ;RTimer :21.333uS 8Bit Input Capture Mode Start(6Mhz)
280
281 8069 E400E4 LDM IRQH,#0 ;Interrut H Request Clear
282 806C E400E5 LDM IRQL,#0 ;Interrut L Request Clear
283
284 806F E438E2 LDM IENH,#0011_1000b ;Enable Remote Falling, Remote Rising, Remote Timer Enable
285 8072 E400E3 LDM IENL,#0000_0000b ;
286
287 8075 E40AEC LDM CKCTLR,#0000_1010b ;BIT INT = 1.3653333mS (@6Mhz)
288 ;Watchdog Clear
289 8078 6F RET
290
291 ;=====;
292 ; Initialize RAM area ;
293 ;=====;
294 Initial_RAM:
295 8079 C4FF LDA #0FFH
296 807B E502 STA rREM_Data
297 807D E500 STA rCUSTOM_1
298 807F E501 STA rCUSTOM_2
299
300 8081 6F RET
301
302
303 ;*****;
304 ; Interrupt Service Routines ;
305 ;*****;

```

```

306
307      ;*****;
308      ; Remote Falling Edge Interrupt Service Routine ;
309      ;*****;
310      Falling_ISP:
311      SAVE
312      @
313      8082 0E      @          PUSH    A
314      8083 2E      @          PUSH    X
315      8084 4E      @          PUSH    Y
316      @
317
318      8085 C504          LDA     rREM_JMP
319      8087 4400          CMP     #0
320      8089 700B          BNE     Falling_ISP_Bye
321
322      808B E42AE7        LDM     RTCR,#0010_1010b ;Remote Timer Stop
323      808E E42BE7        LDM     RTCR,#0010_1011b ;Remote Timer Cleare & Re-Start
324
325      8091 8904          INC     rREM_JMP ;
326      8093 E40003        LDM     rRemoconCNT,#0
327      Falling_ISP_Bye:
328
329      RESTORE
330      @
331      8096 4D      @          POP     Y
332      8097 2D      @          POP     X
333      8098 0D      @          POP     A
334      @
335      8099 7F          RETI
336
337
338      ;*****;
339      ; Remote Rising Edge Interrupt Service Routine ;
340      ;*****;
341      Rising_ISP:
342      ;-----
343      ;SONY Formtat Checking Routine
344      ; Guide+Data(7bit)+Category Code(13bit)
345      ;-----
346      ; Sony Remote Format
347      ; BIT 1 : 1.8msec
348      ; BIT 0 : 1.2msec
349      ; 1mS < BIT 0 < 1.5msec < BIT 1 < 2mS
350      ;-----
351      SAVE
352      @
353      809A 0E      @          PUSH    A
354      809B 2E      @          PUSH    X
355      809C 4E      @          PUSH    Y
356      @
357      809D C5E8          LDA     RTCP0
358      809F E505          STA     rDATA_CAP ;Store Risign Capture Value
359
360      80A1 E42AE7        LDM     RTCR,#0010_1010b ;Remote Timer Stop
361      80A4 E42BE7        LDM     RTCR,#0010_1011b ;Remote Timer Cleare & Re-Start
362
363      80A7 C504          LDA     rREM_JMP
364      80A9 4400          CMP     #00H
365      80AB F007          BEQ     SONY_Rising_err
366      80AD 4401          CMP     #01H

```

```

367 80AF 7007          BNE    Sony_Data_Get    ;Data Check!!
368
369 80B1 1BFF80       JMP    SONY_Header_Check  ;Header Check!!
370
371                SONY_Rising_err:
372 80B4 FF           NOP
373 80B5 1B2481       JMP    REM_CHK_END_1
374
375                Sony_Data_Get:
376 80B8 4C03         TST    rRemoconCNT
377 80BA 7018         BNE    Jmp_Check4_1    ;4ms Over?
378
379 80BC C505         LDA    rDATA_CAP
380
381                SonyDataGet1:
382 80BE 442F         CMP    #47
383 80C0 5012         BCC    Jmp_Check4_1    ;Under 47*21.33=1000usec
384 80C2 445D         CMP    #93
385 80C4 D00E         BCS    Jmp_Check4_1    ;Over 93*21.33=2000usec
386
387 80C6 4446         CMP    #70            ;Under 70*21.33usec=1493usec, bit 0
388                ;If rData_CAP >= 70 CY=1, Not CY=0
389
390 80C8 6906         ROR    rSony_BUF+0    ;LSB First Remocon Data Store
391 80CA 6907         ROR    rSony_BUF+1
392 80CC 6908         ROR    rSony_BUF+2
393
394 80CE D008         BCS    SonyDataGet_Finish ;7+13=20?
395                SonyDataGet2:
396
397                RESTORE
398                @
399 80D0 4D           @        POP    Y
400 80D1 2D           @        POP    X
401 80D2 0D           @        POP    A
402                @
403 80D3 7F           RETI
404
405                Jmp_Check4_1:
406 80D4 FF           NOP
407 80D5 1B0781       JMP    SONY_FMT_Check4_1
408
409                SonyDataGet_Finish:
410 80D8 6906         ROR    rSony_BUF+0
411 80DA 6907         ROR    rSony_BUF+1
412 80DC 6908         ROR    rSony_BUF+2
413
414 80DE 6906         ROR    rSony_BUF+0
415 80E0 6907         ROR    rSony_BUF+1
416 80E2 6908         ROR    rSony_BUF+2
417
418 80E4 6906         ROR    rSony_BUF+0
419 80E6 6907         ROR    rSony_BUF+1
420 80E8 6908         ROR    rSony_BUF+2
421
422 80EA C506         LDA    rSony_BUF+0
423 80EC 841F         AND    #0001_1111B
424 80EE E500         STA    rCUSTOM_1
425
426 80F0 C507         LDA    rSony_BUF+1
427 80F2 E501         STA    rCUSTOM_2
428

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```

429 80F4 6908          ROR    rSony_BUF+2
430 80F6 C508          LDA    rSony_BUF+2
431
432 80F8 847F          AND    #0111_1111B
433 80FA E502          STA    rREM_DATA
434
435 80FC 1B1E81        JMP    REM_RESET    ;END OF DATA
436
437          SONY_Header_Check:
438 80FF 8904          INC    rREM_JMP    ;rREM_JMP = 2
439
440 8101 C505          LDA    rDATA_CAP
441 8103 445E          CMP    #94          ;Under 94*21.33usec=2002usec, Go to Error
442 8105 D003          BCS    SONY_FMT_Check5
443          SONY_FMT_Check4_1:
444
445 8107 1B1E81        JMP    REM_RESET
446
447          SONY_FMT_Check5:
448 810A 4484          CMP    #132         ;Over 132*21.33usec=2815usec, Go to Error
449 810C D0F9          BCS    SONY_FMT_Check4_1
450
451 810E E40806        LDM    rSony_BUF+0,#0000_1000B
452 8111 E40007        LDM    rSony_BUF+1,#0000_0000B
453 8114 E40008        LDM    rSony_BUF+2,#0000_0000B
454
455 8117 E40003        LDM    rRemoconCNT,#0
456
457          RESTORE
458          @
459 811A 4D            @        POP    Y
460 811B 2D            @        POP    X
461 811C 0D            @        POP    A
462          @
463 811D 7F            RETI
464
465          REM_RESET:
466 811E C400          LDA    #00H
467 8120 E505          STA    rDATA_CAP    ; BEFORE CAPTURE DATA
468          REM_CHK_END:
469 8122 E504          STA    rREM_JMP
470          REM_CHK_END_1:
471 8124 E40003        LDM    rRemoconCNT,#0
472          RESTORE
473          @
474 8127 4D            @        POP    Y
475 8128 2D            @        POP    X
476 8129 0D            @        POP    A
477          @
478 812A 7F            RETI
479
480
481
482          ;*****;
483          ; Remote Timer Interrupt Service Routine ;
484          ;*****;
485
486
487          RTimer_ISP:
488          SAVE
489          @
490 812B 0E            @        PUSH   A

```

```

491 812C 2E @ PUSH X
492 812D 4E @ PUSH Y
493 @
494
495 INCR rRemoconCNT,#12,Timer0_ISR_Bye
496 @
497 812E 8903 @ INC rRemoconCNT
498 8130 C503 @ LDA rRemoconCNT
499 8132 440C @ CMP #12
500 8134 7006 @ BNE Timer0_ISR_Bye
501 8136 E40003 @ LDM rRemoconCNT,#0
502 @
503
504 8139 3B4081 CALL Remote_RESET_ALL ;256*21.333 = 5461.333 *12 = 65.071(6Mhz)
505 Timer0_ISR_Bye:
506 RESTORE
507 @
508 813C 4D @ POP Y
509 813D 2D @ POP X
510 813E 0D @ POP A
511 @
512 813F 7F RETI
513
514 Remote_RESET_ALL:
515 8140 C4FF LDA #0FFH
516 8142 E502 STA rREM_Data
517 8144 E500 STA rCUSTOM_1
518 8146 E501 STA rCUSTOM_2
519
520 8148 C400 LDA #00H
521 814A E505 STA rDATA_CAP ; BEFORE CAPTURE DATA
522 814C E504 STA rREM_JMP
523 814E E503 STA rRemoconCNT
524
525 8150 6F RET
526
527 ;-----
528 Not_Used:
529 8151 E438E2 LDM IENH, #0011_1000b ;Enable INT0, INT1, Timer0, Timer1 Enable
530 8154 E400E3 LDM IENL, #0000_0000b ;Enable BIT INT.
531
532 8157 7F RETI
533
534 ORG 0FFDDh ;Unused ROM Area Error
535 FFDD 1B0080 JMP Reset ;Jump Reset
536
537 END ;Program End

```

-- 0 Error(s) --

--- Total Machine Code : 379 Bytes ---