

# VFD Interface

## VFD Module Interface Using GMS87C2020

### INTRODUCTION

The VFD (Vacuum Fluorescent Display) is a kind of triode vacuum tube with three electrodes which are:

- Cathode Filament(s)
- Control Grids
- Illumination Anodes

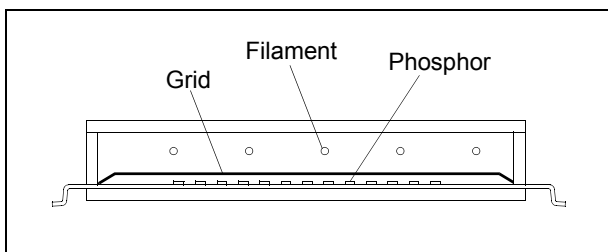


Figure 1. VFD Structure

The electrons emitted from the cathode filaments are controlled by the grids. When the grid is supplied with a positive voltage, it attracts the negative electrons, diffuses them and, due to their acceleration, many flow through the grid mesh towards the anode (opposite charges attract). However, when the grid is supplied with a negative voltage, it repels the negative electrons and prevents them from reaching the anode (similar charges repel).

The illuminating anodes are coated with phosphor which emits light when hit by the electrons. Each anode forms a segment or dot, which collectively form individual characters. When an anode is supplied with a positive voltage, it will attract the electrons which have been accelerated through the grid. The segment emits light when these electrons impact on the phosphor coating. Alternatively when anodes are supplied with a negative voltage, they will repel electrons from their phosphor coating and therefore remain un-illuminated.



Figure 2. VFD Module Form

### VFD DRIVING MODES

Two drive modes are possible with VFD which are referred to as static and multiplexing. The mode is dependent upon the pin-out of the anode segments and grids of the specific VFD.

#### Static Drive

In a static display, each anode segment is individually connected to a lead pin and a single grid covers all the display pattern in the VFD. This has the advantage in that it only requires 10 to 15 volts DC to illuminate the display and, in some cases, illumination is possible using standard 12 volts C-MOS logic. The major disadvantage with static mode is the need for more lead pins and IC drivers as the number of anode segments increases. Figure 3 and Figure 4 show the basic construction and drive circuit.

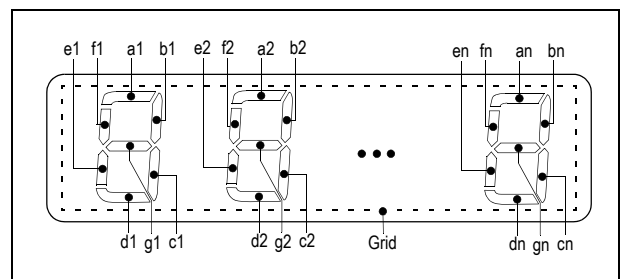


Figure 3. Static Drive VFD

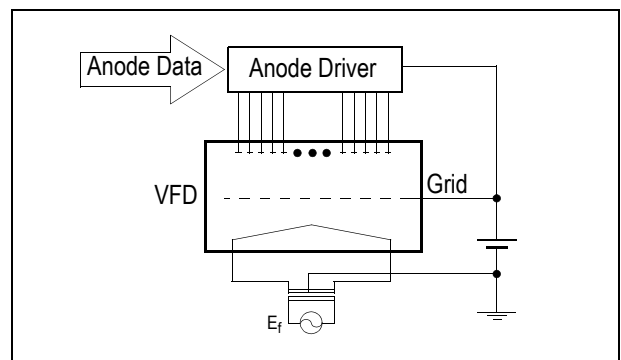


Figure 4. Driving Circuit of Static Drive VFD

#### Dynamic Drive

To minimize the number of pin connections and driver chips, the majority of VFD's use the dynamic drive method. As shown in Figure 5, corresponding anode segments are connected in common under each separate grid, with each in turn being connected to a data line. Each

character has its own separate grid which not only diffuses the electrons from the filaments, but also controls the selection of the character position in a “time sharing method” dynamic cycle. The duty cycle 'on time' of each character will determine the appropriate operating voltage required to provide sufficient luminance. Figure 6 shows the basic dynamic driving circuit.

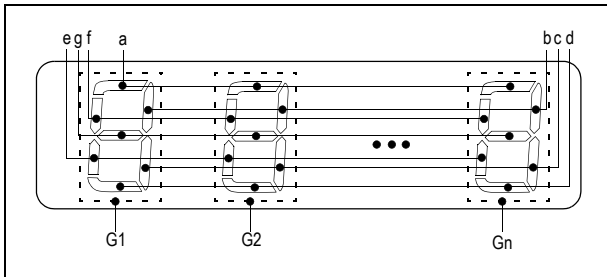


Figure 5. Dynamic Drive VFD

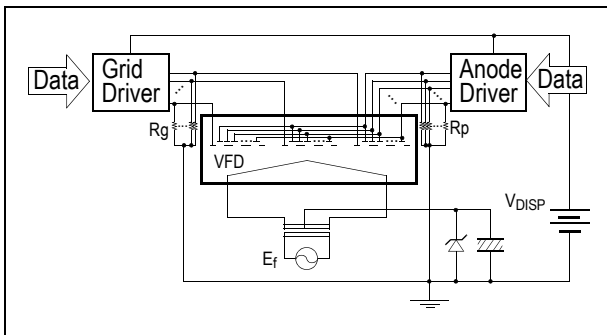


Figure 6. Driving Circuit of Dynamic Drive VFD

### BRIGHTNESS CONTROL (DIMMING)

High brightness is the main characteristic of VFD. However, in certain applications, it may be desirable to offer dimming capabilities for operation in dark environments. In such a case, the brightness level can be controlled by reducing the duty factor as shown in Figure 7. The brightness level can be adjusted in proportion to the luminous ‘on’ time to ‘off’ time. However brightness dimming by reduction of filament voltage or anode/grid voltage is not recommended because this may cause uneven illumina-

tion.

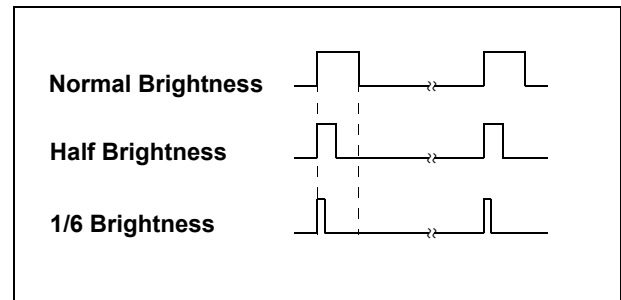


Figure 7. Pulse Width Reduction

### HARDWARE CONNECTION

Figure 9 is the circuit diagram for a front panel system of DVDP. Normally the voltage to be supplied at VFD module is approximately 12V to 40V depending on size and display form (Static: above 12V, Dynamic; above 30V) and bias voltage for heating filament is 2V to 6V .

In this application, we selected GMS87C2020 microcontroller built in high voltage port and 4MHz oscillator.

Also the negative voltage is applied to the circuit ( $V_{DD} = 0V$ ,  $V_{SS} = -5V$ ,  $V_{DISP} = -26V$ ). Pull-down resistors (47k $\Omega$ ) are attached to high-voltage pins to supply  $V_{DISP}$  voltage (Mask Option).

### SOFTWARE CONNECTION

The example program is listed in Appendix A.

It expresses 12 patterns to VFD panel every 400ms according to the period of Basic Interval Timer (1.024ms).

Each pattern is constructed to 16 x 8 matrix according as the size of VFD module.

The flow of display form is as follows.

- **The beginning block : All segment is ON.**
- **The middle blocks :**  
 The numbers are increased one by one at 7segment and the each segment is turned on in order.
- **The last block : All segment is OFF.**

Each matrix is composed of 16 x 8 bits structure and can be modified easily because of using indirect addressing mode and ROM patterns.

To change the period of patterns, we can manipulate the number related period at Basic Interval Timer Interrupt Routine or the label of of “TimeCheck:”

**Example:** 1.024ms x 196 = 200.704ms  
 200.704ms x 2 = 401.408ms

CIRCUIT DIAGRAM

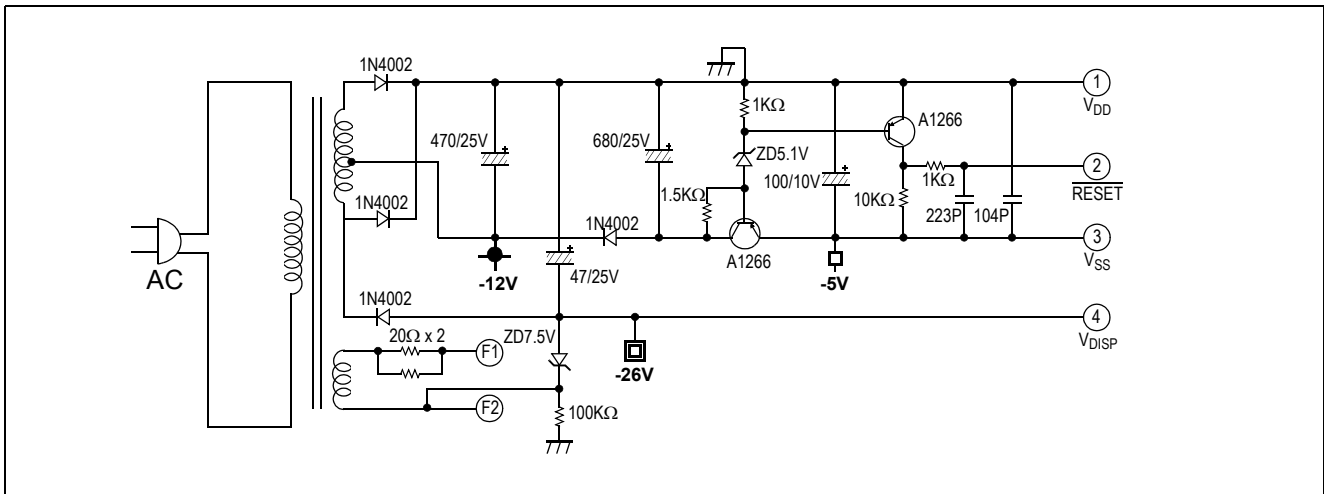


Figure 8. Power Source Circuit Diagram

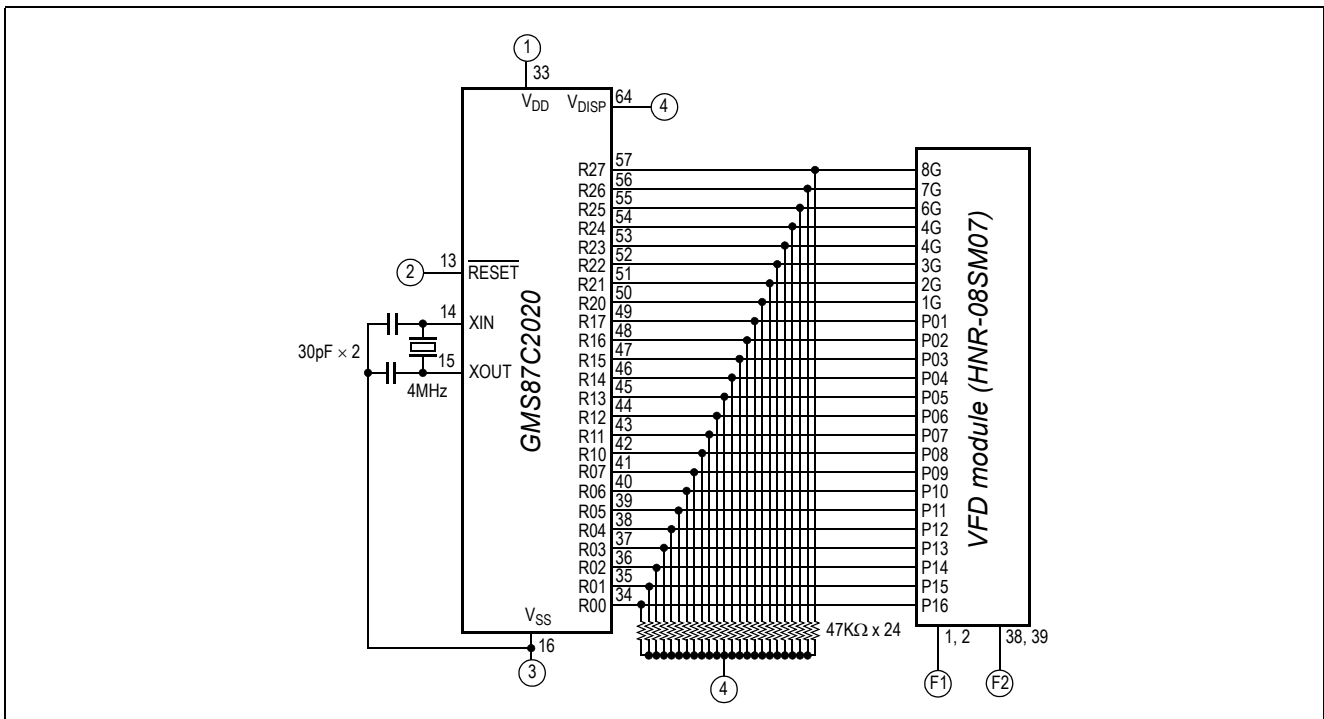


Figure 9. Simple Hardware Connection

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## Appendix A:

GMS800 series MICOM ASSEMBLER Thu Jan 20 14:19:23 2005  
(PAGE 1)

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1          PAGE      1000
2          ;*****
3          ;Company   : MagnaChip Semiconductor MCU Application Team
4          ;Programmer: Harris Hwang
5          ;-----
6          ;TITLE     : VFD Module(for DVDP panel) Test Program
7          ;Device    : GMS87C2020
8          ;OSC       : 4MHz
9          ;START     : 2005.01. ~ 2005.01.
10         ;*****
11         ;
12         ;** Peripheral Register
13         R0         EQU      0C0H          ;port R0 register(R/W)
14         R0IO      EQU      0C1H          ;port R0 data I/O direction register(W)
15         R1         EQU      0C2H          ;port R1 register(R/W)
16         R1IO      EQU      0C3H          ;port R1 data I/O direction register(W)
17         R2         EQU      0C4H          ;port R2 register(R/W)
18         R2IO      EQU      0C5H          ;port R2 data I/O direction register(W)
19         R3         EQU      0C6H          ;port R3 register(R/W)
20         R3IO      EQU      0C7H          ;port R3 data I/O direction register(W)
21         R4         EQU      0C8H          ;port R4 register(R/W)
22         R4IO      EQU      0C9H          ;port R4 data I/O direction register(W)
23         R5         EQU      0CAH          ;port R5 register(R/W)
24         R5IO      EQU      0CBH          ;port R5 data I/O direction register(W)
25         R6         EQU      0CCH          ;Port R6 Register(R/W)
26         R6IO      EQU      0CDH          ;Port R6 Data I/O Direction Register(W)
27         R7         EQU      0CEH          ;Port R7 Register(R/W)
28         R7IO      EQU      0CFH          ;Port R7 Data I/O Direction Register(W)
29         ;
30         TM0        EQU      0D0H          ;Timer0 Mode Control Register(R/W)
31         TOST        EQU      0,0D0H      ;Timer0 Start bit
32         T0          EQU      0D1H          ; (R)
33         TDR0        EQU      0D1H          ; (W)
34         CDR0        EQU      0D1H          ; (R)
35         TM1         EQU      0D2H          ;Timer1 Mode Control Register(R/W)
36         TDR1        EQU      0D3H          ; (W)
37         T1PPR       EQU      0D3H          ; (W)
38         T1          EQU      0D4H          ; (R)
39         CDR1        EQU      0D4H          ; (R)
40         T1PDR       EQU      0D4H          ; (R/W)
41         PWM1HR      EQU      0D5H          ;Timer1 PWM High Register(W)
42         BUR         EQU      0DEH          ;Buzzer Driver Register(W)
43         SIOM        EQU      0E0H          ;SPI Mode Control Register(R/W)
44         SIOR        EQU      0E1H          ;SPI Data Shift Register(R/W)
45         IENH        EQU      0E2H          ;Interrupt Enable Register High(R/W)
46         IENL        EQU      0E3H          ;Interrupt Enable Register Low(R/W)
47         IRQH        EQU      0E4H          ;Interrupt Request Flag Register High(R/W)
48         IRQL        EQU      0E5H          ;Interrupt Request Flag Register Low(R/W)
49         IEDS        EQU      0E6H          ;External Interrupt Edge Selection Register(R/W)
50         ADCM        EQU      0EAH          ;A/D Converter Mode Register(R/W, bit0 is R)
51         ADCR        EQU      0EBh          ;A/D Converter Result Register(R)
52         BITR        EQU      0ECh          ;Basic Interval Timer Register(R)
53         CKCTLR      EQU      0ECh          ;** (W)
54         WDTR        EQU      0EDh          ;Watch Dog Timer Register(W)
55         ;** (R);The current count value is read.
56         PFDR        EQU      0EFh          ;PDF Control Register(R/W)
57         R0FUNC      EQU      0F4h          ;R0 Port Function Selection Register(W)
58         R4FUNC      EQU      0F5h          ;R4 Port Function Selection Register(W)

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59      R5FUNC EQU    0F6h      ;R5 Port Function Selection Register(W)
60      R6FUNC EQU    0F7h      ;R6 Port Function Selection Register(W)
61      R7FUNC EQU    0F8h      ;R6 Port Function Selection Register(W)
62      R5NODR EQU    0F9h      ;R5 Port N-MOS Open Drain Selection Register(W)
63      SCMR EQU     0FAh      ;System Clock Mode Register (R/W)
64      RA EQU     0FBh      ;RA Port Data Register(R)
65      RA0 EQU     0,0FBh     ;1-bit high voltage input only port.
66      ;
67      ;** User Memory (RAM)
68      VFD_P1_P8 DS      8
69      VFD_P9_P16 DS     8
70      COUNT_200MS DS    1
71      COUNT_1SEC DS     1
72      COUNT_PATTERN DS   1
73      WORK DS          2      ; (WORK+1) (WORK)
74      SCAN_CNT DS       1
75      ;
76      FLAG DS          1
77      FLAG_200MS_OVER EQU    0,FLAG
78      ;
79      ;** Port Definition
80      SCAN_PORT EQU     R2
81      P1_P8_PORT EQU    R1      ;P1 (bit7), P2, P3, P4, P5, P6, P7, P8 (bit0)
82      P9_P16_PORT EQU   R0      ;P9 (bit7), P10, P11, P12, P13, P14, P15, P16 (bit0)
83      ;
84      ;** MACRO **
85      SAVE MACRO          ;reg. save
86          PUSH A
87          PUSH X
88          PUSH Y
89      ENDM
90      RESTORE MACRO      ;reg. restore
91          POP Y
92          POP X
93          POP A
94      ENDM
95      ;** Vector Table
96
97          ORG    0FFE6H
98 FFE6 ADD0          DW    BasicTimer ; Basic Interval Timer(1.024ms)
99          ORG    0FFFEH
100 FFFE 00D0         DW    Reset      ; Reset
101      ;-----
102      ;** Program Start
103      ;-----
104          ORG    0D000h      ;0B000H(20K),0D000H(12K) Program Start Address
105      Reset:
106 D000 60           di          ;Min.InstructionCycle=1us@4MHZ
107 D001 40           clrg
108 D002 1EFF         ldx    #0FFh    ;Stack Pointer=0FFh(GMS87C2012/20)
109 D004 8E           txsp
110      ;-- RAM CLEAR -----
111 D005 1E00         ldx    #0      ;0Page RAM Clear(00h ~ BFh)
112      Clr0Page:
113 D007 C400         lda    #0
114 D009 FB           sta    {X}+
115 D00A 5EC0         cmpx  #0c0h
116 D00C 70F9         bne   Clr0Page
117      ;---
118 D00E 3B17D0       call  Initial    ;I/O, Register Initial
119
120 D011 E0           ei

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121          Main:
122 D012 3B72D0          call    !TimeCheck
123 D015 2FFB           bra     Main
124          ;*****
125          ;
126          ;-----
127          ;** Sub Routine
128          ;-----
129          ;-- Initial I/O PORT
130          Initial:
131 D017 E400C0          ldm     R0,#0000_0000b
132 D01A E4FFC1          ldm     R0IO,#1111_1111b ;R07, P09 data display (Output-High)
133          ;R06, P10 data display (Output-High)
134          ;R05, P11 data display (Output-High)
135          ;R04, P12 data display (Output-High)
136          ;R03, P13 data display (Output-High)
137          ;R02, P14 data display (Output-High)
138          ;R01, P15 data display (Output-High)
139          ;R00, P16 data display (Output-High)
140 D01D E400C2          ldm     R1,#0000_0000b
141 D020 E4FFC3          ldm     R1IO,#1111_1111b ;R17, P01 data display (Output-High)
142          ;R16, P02 data display (Output-High)
143          ;R15, P03 data display (Output-High)
144          ;R14, P04 data display (Output-High)
145          ;R13, P05 data display (Output-High)
146          ;R12, P06 data display (Output-High)
147          ;R11, P07 data display (Output-High)
148          ;R10, P08 data display (Output-High)
149 D023 E400C4          ldm     R2,#0000_0000b
150 D026 E4FFC5          ldm     R2IO,#1111_1111b ;R27, 8G data display (Output-High)
151          ;R26, 7G data display (Output-High)
152          ;R25, 6G data display (Output-High)
153          ;R24, 5G data display (Output-High)
154          ;R03, 4G data display (Output-High)
155          ;R22, 3G data display (Output-High)
156          ;R21, 2G data display (Output-High)
157          ;R20, 1G data display (Output-High)
158 D029 E400C6          ldm     R3,#0
159 D02C E4FFC7          ldm     R3IO,#0FFh
160 D02F E400C8          ldm     R4,#0
161 D032 E4FFC9          ldm     R4IO,#0FFh
162 D035 E400CA          ldm     R5,#0
163 D038 E4FFCB          ldm     R5IO,#0FFh
164 D03B E400CC          ldm     R6,#0
165 D03E E4FFCD          ldm     R6IO,#0FFh
166 D041 E400CE          ldm     R7,#0
167 D044 E4FFCF          ldm     R7IO,#0FFh
168 D047 E400F4          ldm     R0FUNC,#0
169 D04A E400F5          ldm     R4FUNC,#0
170 D04D E400F6          ldm     R5FUNC,#0
171 D050 E400F9          ldm     R5NODR,#0
172 D053 E400F7          ldm     R6FUNC,#0
173 D056 E400F8          ldm     R7FUNC,#0
174          ;
175 D059 E409EC          ldm     ckctlr,#0000_1001b ;BIT=4x256=1024us(1/(4Mhz/16)=4us)
176 D05C E400E2          ldm     IENH,#0
177 D05F E420E3          ldm     IENL,#0010_0000b ;BIT enable
178 D062 E400E4          ldm     IRQH,#0
179 D065 E400E5          ldm     IRQL,#0
180          ;no use-- TM0,TDR0,TM1,TDR1,T1PDR,PWM1HR,BUR,SIOM,SIOR,IEDS,ADCM,wdr,pfdr,scmr
181          ;use -- ckctlr,ienh,ienl,irqh,irql,ra
182          ;-- Initial Data

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183 D068 1E00          ldx    #VFD_P1_P8
184          InitialTotalON:
185 D06A C4FF          lda    #0FFh
186 D06C FB            sta    {X}+
187 D06D 5E11          cmpx  #17
188 D06F 70F9          bne   InitialTotalON
189
190 D071 6F            ret
191          ;-- Time Check
192          TimeCheck:
193 D072 131610         BBC    FLAG_200MS_OVER,TimeCheckEnd
194 D075 1116          clr1  FLAG_200MS_OVER ;Every 200ms
195 D077 8911          inc   COUNT_1SEC
196 D079 C511          lda   COUNT_1SEC
197 D07B 4402          CMP   #2 ;200ms*5=1000ms=1sec.
198 D07D 7006          bne   TimeCheckEnd ;200ms*2=400ms
199          ;-- Data Conversion after 1sec.
200 D07F E40011        ldm   COUNT_1SEC,#0 ;Every 1sec.
201          ;set1 FLAG_1SEC_OVER
202          ;BBC FLAG_1SEC_OVER,TimeCheckEnd
203          ;clr1 FLAG_1SEC_OVER
204 D082 3B86D0        CALL  !ChangeDisplyData ;Input Dispaly data at VFD_P1_P8,VFD_P9_P16.
205          TimeCheckEnd:
206 D085 6F            ret
207
208          ;-- 1sec. routine
209          ChangeDisplyData:
210 D086 8912          inc   COUNT_PATTERN
211 D088 C512          lda   COUNT_PATTERN
212 D08A 440D          cmp   #0Dh
213 D08C 7003          bne   ChangePattern
214 D08E E40112        ldm   COUNT_PATTERN,#1 ;1h~13h, "0" is inhibited.
215          ChangePattern:
216 D091 C512          lda   COUNT_PATTERN
217 D093 A8            dec   A
218 D094 08            asl   A
219 D095 9F            tay   ;if1,Y=0, if2,Y=2, if3,Y=4, if4,Y=6, if1,Y=0
220 D096 D5E9D0        lda   !Pattern+Y ;//Y=0~4
221 D099 E513          sta   WORK ;//Work DS 2
222 D09B D5EAD0        lda   !Pattern+1+Y ;//
223 D09E E514          sta   WORK+1 ;//
224 D0A0 3E00          ldy   #0
225          StoreTo16bytes:
226 D0A2 D713          lda   [WORK]+Y ;//16bytes data conversion.
227 D0A4 F50000        sta   !VFD_P1_P8+Y ;VFD_P1_P8 ~ VFD_P9_P16
228 D0A7 9E            inc   Y
229 D0A8 7E10          cmpy  #16
230 D0AA 70F6          bne   StoreTo16bytes
231          ChangeDisplyDataEnd:
232 D0AC 6F            ret
233
234          ;-----
235          ;** Interrupt Routine
236          ;-----
237          BasicTimer:
238          SAVE
239 D0AD 0E            @    PUSH  A
240 D0AE 2E            @    PUSH  X
241 D0AF 4E            @    PUSH  Y
242          ;-- Display
243 D0B0 E400C2        ldm   P1_P8_PORT,#0 ;VFD Data Port OFF
244 D0B3 E400C0        ldm   P9_P16_PORT,#0 ;VFD Data Port OFF

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245 D0B6 E400C4      ldm    SCAN_PORT,#0    ;VFD Scan Port OFF
246                ;
247 D0B9 8915        inc    SCAN_CNT
248 D0BB C515        lda    SCAN_CNT
249 D0BD 8407        and    #0000_0111b    ;A = A and #0000_0111b
250 D0BF E515        sta    SCAN_CNT
251 D0C1 9F          TAY                ;Y=0~7(1,2,3.. 6,7,0,1,...)
252                ;
253 D0C2 D50000      lda    !VFD_P1_P8+Y
254 D0C5 E5C2        sta    P1_P8_PORT
255 D0C7 D50800      lda    !VFD_P9_P16+Y
256 D0CA E5C0        sta    P9_P16_PORT
257                ;
258 D0CC D5E1D0      lda    !Strobe+Y
259 D0CF E5C4        sta    SCAN_PORT
260                ;
261 D0D1 8910        inc    COUNT_200MS
262 D0D3 C510        lda    COUNT_200MS
263 D0D5 44C4        cmp    #196            ;1.024ms*196=200.704ms
264 D0D7 7005        bne    BasicTimerEnd
265 D0D9 E40010      ldm    COUNT_200MS,#0
266 D0DC 0116        set1   FLAG_200MS_OVER
267                BasicTimerEnd:
268                RESTORE
269 D0DE 4D          @      POP    Y
270 D0DF 2D          @      POP    X
271 D0E0 0D          @      POP    A
                reti
272                ;-----
273                Strobe:
274 D0E1 01          DB     00000001b    ; (1G)
275 D0E2 02          DB     00000010b    ; (2G)
276 D0E3 04          DB     00000100b    ; (3G)
277 D0E4 08          DB     00001000b    ; (4G)
278 D0E5 10          DB     00010000b    ; (5G)
279 D0E6 20          DB     00100000b    ; (6G)
280 D0E7 40          DB     01000000b    ; (7G)
281 D0E8 80          DB     10000000b    ; (8G)
282                ;*****
283                Pattern:
284 D0E9 03D1        DW     Form1            ;Y=1 (0,1)
285 D0EB 13D1        DW     Form2            ;Y=2 (2,3)
286 D0ED 23D1        DW     Form3            ;Y=3 (4,5)
287 D0EF 33D1        DW     Form4            ;Y=4 (6,7)
288 D0F1 43D1        DW     Form5            ;Y=5 (8,9)
289 D0F3 53D1        DW     Form6            ;Y=6 (A,B)
290 D0F5 63D1        DW     Form7            ;Y=7 (C,D)
291 D0F7 73D1        DW     Form8            ;Y=8 (E,F)
292 D0F9 83D1        DW     Form9            ;Y=9 (10h,11h)
293 D0FB 93D1        DW     Form10           ;Y=A (12h,13h)
294 D0FD A3D1        DW     Form11           ;Y=B (14h,15h)
295 D0FF B3D1        DW     Form12           ;Y=C (16h,17h)
296 D101 FF         nop
297 D102 FF         nop
298                ;-----
299                ;To add Pattern
300                ;1. To Pattern: Add DW Form5,Form6,..
301                ;2. Add The data of Form5,7..
302                ;3. Write the number with 1 greater than that of pattern at "cmp #5"
303                ;   of The label of ChangeDisplyData:
304                ;-----
305                Form1:

```

```

306          ;p1,p2,p3,p4_p5,p6,p7,p8
307 D103 40          DB          0100_0000b  ;1G(p1/R17)-> VFD_P1_P8
308 D104 63          DB          0110_0011b  ;(H);2G(p2/R16)
309 D105 00          DB          0000_0000b  ;3G(p3/R15)
310 D106 00          DB          0000_0000b  ;4G(p4/R14)
311 D107 00          DB          0000_0000b  ;5G(p5/R13)
312 D108 9F          DB          1001_1111b  ;6G(p6/R12)
313 D109 48          DB          0100_1000b  ;7G(p7/R11)
314 D10A 80          DB          1000_0000b  ;8G(p8/R10)
315          ;p9,p10,p11,p12_p13,p14,p15,p16
316 D10B 51          DB          0101_0001b  ;1G(p9/R07)->VFD_P9_P16
317 D10C 18          DB          0001_1000b  ;(H);2G(p10/R06)
318 D10D 00          DB          0000_0000b  ;3G(p11/R05)
319 D10E 00          DB          0000_0000b  ;4G(p12/R04)
320 D10F 01          DB          0000_0001b  ;5G(p13/R03)
321 D110 0A          DB          0000_1010b  ;6G(p14/R02)
322 D111 8A          DB          1000_1010b  ;7G(p15/R01)
323 D112 8A          DB          1000_1010b  ;8G(p16/R00)
324          Form2:
325          ;p1,p2,p3,p4_p5,p6,p7,p8
326 D113 C3          DB          1100_0011b  ;1G(p1/R17)-> VFD_P1_P8
327 D114 63          DB          0110_0011b  ;(Y);2G(p2/R16)
328 D115 63          DB          0110_0011b  ;(H);3G(p3/R15)
329 D116 00          DB          0000_0000b  ;4G(p4/R14)
330 D117 00          DB          0000_0000b  ;5G(p5/R13)
331 D118 3F          DB          0011_1111b  ;6G(p6/R12)
332 D119 D7          DB          1101_0111b  ;7G(p7/R11)
333 D11A 71          DB          0111_0001b  ;8G(p8/R10)
334          ;p9,p10,p11,p12_p13,p14,p15,p16
335 D11B 4D          DB          0100_1101b  ;1G(p9/R07)->VFD_P9_P16
336 D11C 40          DB          0100_0000b  ;(Y);2G(p10/R06)
337 D11D 18          DB          0001_1000b  ;(H);3G(p11/R05)
338 D11E 00          DB          0000_0000b  ;4G(p12/R04)
339 D11F 01          DB          0000_0001b  ;5G(p13/R03)
340 D120 0A          DB          0000_1010b  ;6G(p14/R02)
341 D121 97          DB          1001_0111b  ;7G(p15/R01)
342 D122 97          DB          1001_0111b  ;8G(p16/R00)
343          Form3:
344          ;p1,p2,p3,p4_p5,p6,p7,p8
345 D123 C5          DB          1100_0101b  ;1G(p1/R17)-> VFD_P1_P8
346 D124 70          DB          0111_0000b  ;(N);2G(p2/R16)
347 D125 63          DB          0110_0011b  ;(Y);3G(p3/R15)
348 D126 63          DB          0110_0011b  ;(H);4G(p4/R14)
349 D127 00          DB          0000_0000b  ;5G(p5/R13)
350 D128 5F          DB          0101_1111b  ;6G(p6/R12)
351 D129 DB          DB          1101_1011b  ;7G(p7/R11)
352 D12A 15          DB          0001_0101b  ;8G(p8/R10)
353          ;p9,p10,p11,p12_p13,p14,p15,p16
354 D12B 55          DB          0101_0101b  ;1G(p9/R07)->VFD_P9_P16
355 D12C 38          DB          0011_1000b  ;(N);2G(p10/R06)
356 D12D 40          DB          0100_0000b  ;(Y);3G(p11/R05)
357 D12E 18          DB          0001_1000b  ;(H);4G(p12/R04)
358 D12F 01          DB          0000_0001b  ;5G(p13/R03)
359 D130 0A          DB          0000_1010b  ;6G(p14/R02)
360 D131 9B          DB          1001_1011b  ;7G(p15/R01)
361 D132 9B          DB          1001_1011b  ;8G(p16/R00)
362          Form4:
363          ;p1,p2,p3,p4_p5,p6,p7,p8
364 D133 61          DB          0110_0001b  ;1G(p1/R17)-> VFD_P1_P8
365 D134 88          DB          1000_1000b  ;(I);2G(p2/R16)
366 D135 70          DB          0111_0000b  ;(N);3G(p3/R15)
367 D136 63          DB          0110_0011b  ;(Y);4G(p4/R14)

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368 D137 63          DB      0110_0011b   ; (H) ; 5G (p5/R13)
369 D138 9F          DB      1001_1111b   ; 6G (p6/R12)
370 D139 78          DB      0111_1000b   ; 7G (p7/R11)
371 D13A 12          DB      0001_0010b   ; 8G (p8/R10)
372                ;p9,p10,p11,p12_p13,p14,p15,p16
373 D13B D1          DB      1101_0001b   ; 1G (p9/R07) ->VFD_P9_P16
374 D13C 44          DB      0100_0100b   ; (I) ; 2G (p10/R06)
375 D13D 38          DB      0011_1000b   ; (N) ; 3G (p11/R05)
376 D13E 40          DB      0100_0000b   ; (Y) ; 4G (p12/R04)
377 D13F 19          DB      0001_1001b   ; (H) ; 5G (p13/R03)
378 D140 0A          DB      0000_1010b   ; 6G (p14/R02)
379 D141 DA          DB      1101_1010b   ; 7G (p15/R01)
380 D142 DA          DB      1101_1010b   ; 8G (p16/R00)
381                Form5:
382                ;p1,p2,p3,p4_p5,p6,p7,p8
383 D143 A3          DB      1010_0011b   ; 1G (p1/R17) -> VFD_P1_P8
384 D144 14          DB      0001_0100b   ; (X) ; 2G (p2/R16)
385 D145 88          DB      1000_1000b   ; (I) ; 3G (p3/R15)
386 D146 70          DB      0111_0000b   ; (N) ; 4G (p4/R14)
387 D147 63          DB      0110_0011b   ; (Y) ; 5G (p5/R13)
388 D148 3F          DB      0011_1111b   ; 6G (p6/R12)
389 D149 BB          DB      1011_1011b   ; 7G (p7/R11)
390 D14A 91          DB      1001_0001b   ; 8G (p8/R10)
391                ;p9,p10,p11,p12_p13,p14,p15,p16
392 D14B 55          DB      0101_0101b   ; 1G (p9/R07) ->VFD_P9_P16
393 D14C A0          DB      1010_0000b   ; (X) ; 2G (p10/R06)
394 D14D 44          DB      0100_0100b   ; (I) ; 3G (p11/R05)
395 D14E 38          DB      0011_1000b   ; (N) ; 4G (p12/R04)
396 D14F 41          DB      0100_0001b   ; (Y) ; 5G (p13/R03)
397 D150 0A          DB      0000_1010b   ; 6G (p14/R02)
398 D151 5B          DB      0101_1011b   ; 7G (p15/R01)
399 D152 5B          DB      0101_1011b   ; 8G (p16/R00)
400                Form6:
401                ;p1,p2,p3,p4_p5,p6,p7,p8
402 D153 25          DB      0010_0101b   ; 1G (p1/R17) -> VFD_P1_P8
403 D154 00          DB      0000_0000b   ; 2G (p2/R16)
404 D155 14          DB      0001_0100b   ; (X) ; 3G (p3/R15)
405 D156 88          DB      1000_1000b   ; (I) ; 4G (p4/R14)
406 D157 70          DB      0111_0000b   ; (N) ; 5G (p5/R13)
407 D158 50          DB      0101_0000b   ; 6G (p6/R12)
408 D159 3E          DB      0011_1110b   ; 7G (p7/R11)
409 D15A 70          DB      0111_0000b   ; 8G (p8/R10)
410                ;p9,p10,p11,p12_p13,p14,p15,p16
411 D15B 5D          DB      0101_1101b   ; 1G (p9/R07) ->VFD_P9_P16
412 D15C 00          DB      0000_0000b   ; 2G (p10/R06)
413 D15D A0          DB      1010_0000b   ; (X) ; 3G (p11/R05)
414 D15E 44          DB      0100_0100b   ; (I) ; 4G (p12/R04)
415 D15F 39          DB      0011_1001b   ; (N) ; 5G (p13/R03)
416 D160 E9          DB      1110_1001b   ; 6G (p14/R02)
417 D161 5F          DB      0101_1111b   ; 7G (p15/R01)
418 D162 5F          DB      0101_1111b   ; 8G (p16/R00)
419                Form7:
420                ;p1,p2,p3,p4_p5,p6,p7,p8
421 D163 C0          DB      1100_0000b   ; 1G (p1/R17) -> VFD_P1_P8
422 D164 74          DB      0111_0100b   ; (M) ; 2G (p2/R16)
423 D165 00          DB      0000_0000b   ; 3G (p3/R15)
424 D166 14          DB      0001_0100b   ; (X) ; 4G (p4/R14)
425 D167 88          DB      1000_1000b   ; (I) ; 5G (p5/R13)
426 D168 90          DB      1001_0000b   ; 6G (p6/R12)
427 D169 C9          DB      1100_1001b   ; 7G (p7/R11)
428 D16A 05          DB      0000_0101b   ; 8G (p8/R10)
429                ;p9,p10,p11,p12_p13,p14,p15,p16

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430 D16B D1          DB      1101_0001b   ;1G(p9/R07)->VFD_P9_P16
431 D16C 58          DB      0101_1000b   ;(M);2G(p10/R06)
432 D16D 00          DB      0000_0000b   ;3G(p11/R05)
433 D16E A0          DB      1010_0000b   ;(X);4G(p12/R04)
434 D16F 45          DB      0100_0101b   ;(I);5G(p13/R03)
435 D170 E9          DB      1110_1001b   ;6G(p14/R02)
436 D171 8A          DB      1000_1010b   ;7G(p15/R01)
437 D172 8A          DB      1000_1010b   ;8G(p16/R00)
438
439 Form8:
440 ;p1,p2,p3,p4_p5,p6,p7,p8
440 D173 E3          DB      1110_0011b   ;1G(p1/R17)-> VFD_P1_P8
441 D174 A0          DB      1010_0000b   ;(C);2G(p2/R16)
442 D175 74          DB      0111_0100b   ;(M);3G(p3/R15)
443 D176 00          DB      0000_0000b   ;4G(p4/R14)
444 D177 14          DB      0001_0100b   ;(X);5G(p5/R13)
445 D178 30          DB      0011_0000b   ;6G(p6/R12)
446 D179 FF          DB      1111_1111b   ;7G(p7/R11)
447 D17A 13          DB      0001_0011b   ;8G(p8/R10)
448 ;p9,p10,p11,p12_p13,p14,p15,p16
449 D17B 5D          DB      0101_1101b   ;1G(p9/R07)->VFD_P9_P16
450 D17C 0C          DB      0000_1100b   ;(C);2G(p10/R06)
451 D17D 58          DB      0101_1000b   ;(M);3G(p11/R05)
452 D17E 00          DB      0000_0000b   ;4G(p12/R04)
453 D17F A1          DB      1010_0001b   ;(X);5G(p13/R03)
454 D180 E9          DB      1110_1001b   ;6G(p14/R02)
455 D181 DF          DB      1101_1111b   ;7G(p15/R01)
456 D182 DF          DB      1101_1111b   ;8G(p16/R00)
457
458 Form9:
459 ;p1,p2,p3,p4_p5,p6,p7,p8
459 D183 E5          DB      1110_0101b   ;1G(p1/R17)-> VFD_P1_P8
460 D184 60          DB      0110_0000b   ;(U);2G(p2/R16)
461 D185 A0          DB      1010_0000b   ;(C);3G(p3/R15)
462 D186 74          DB      0111_0100b   ;(M);4G(p4/R14)
463 D187 00          DB      0000_0000b   ;5G(p5/R13)
464 D188 50          DB      0101_0000b   ;6G(p6/R12)
465 D189 F9          DB      1111_1001b   ;7G(p7/R11)
466 D18A 91          DB      1001_0001b   ;8G(p8/R10)
467 ;p9,p10,p11,p12_p13,p14,p15,p16
468 D18B 51          DB      0101_0001b   ;1G(p9/R07)->VFD_P9_P16
469 D18C 1C          DB      0001_1100b   ;(U);2G(p10/R06)
470 D18D 0C          DB      0000_1100b   ;(C);3G(p11/R05)
471 D18E 58          DB      0101_1000b   ;(M);4G(p12/R04)
472 D18F 01          DB      0000_0001b   ;5G(p13/R03)
473 D190 E9          DB      1110_1001b   ;6G(p14/R02)
474 D191 DA          DB      1101_1010b   ;7G(p15/R01)
475 D192 DA          DB      1101_1010b   ;8G(p16/R00)
476
477 Form10:
478 ;p1,p2,p3,p4_p5,p6,p7,p8
478 D193 E4          DB      1110_0100b   ;1G(p1/R17)-> VFD_P1_P8
479 D194 00          DB      0000_0000b   ;2G(p2/R16)
480 D195 60          DB      0110_0000b   ;(U);3G(p3/R15)
481 D196 A0          DB      1010_0000b   ;(C);4G(p4/R14)
482 D197 74          DB      0111_0100b   ;(M);5G(p5/R13)
483 D198 90          DB      1001_0000b   ;6G(p6/R12)
484 D199 EF          DB      1110_1111b   ;7G(p7/R11)
485 D19A 61          DB      0110_0001b   ;8G(p8/R10)
486 ;p9,p10,p11,p12_p13,p14,p15,p16
487 D19B DD          DB      1101_1101b   ;1G(p9/R07)->VFD_P9_P16
488 D19C 00          DB      0000_0000b   ;2G(p10/R06)
489 D19D 1C          DB      0001_1100b   ;(U);3G(p11/R05)
490 D19E 0C          DB      0000_1100b   ;(C);4G(p12/R04)
491 D19F 59          DB      0101_1001b   ;(M),P16 ;5G(p13/R03)

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492 D1A0 E9          DB      1110_1001b  ;6G(p14/R02)
493 D1A1 CF          DB      1100_1111b  ;7G(p15/R01)
494 D1A2 CF          DB      1100_1111b  ;8G(p16/R00)
495
496                Form11:
                    ;p1,p2,p3,p4_p5,p6,p7,p8
497 D1A3 FF          DB      1111_1111b  ;1G(p1/R17)-> VFD_P1_P8
498 D1A4 FF          DB      1111_1111b  ;2G(p2/R16)
499 D1A5 FF          DB      1111_1111b  ;3G(p3/R15)
500 D1A6 FF          DB      1111_1111b  ;4G(p4/R14)
501 D1A7 FF          DB      1111_1111b  ;5G(p5/R13)
502 D1A8 FF          DB      1111_1111b  ;6G(p6/R12)
503 D1A9 FF          DB      1111_1111b  ;7G(p7/R11)
504 D1AA FF          DB      1111_1111b  ;8G(p8/R10)
505                ;p9,p10,p11,p12_p13,p14,p15,p16
506 D1AB FF          DB      1111_1111b  ;1G(p9/R07)->VFD_P9_P16
507 D1AC FF          DB      1111_1111b  ;2G(p10/R06)
508 D1AD FF          DB      1111_1111b  ;3G(p11/R05)
509 D1AE FF          DB      1111_1111b  ;4G(p12/R04)
510 D1AF FF          DB      1111_1111b  ;5G(p13/R03)
511 D1B0 FF          DB      1111_1111b  ;6G(p14/R02)
512 D1B1 FF          DB      1111_1111b  ;7G(p15/R01)
513 D1B2 FF          DB      1111_1111b  ;8G(p16/R00)
514
515                Form12:
                    ;p1,p2,p3,p4_p5,p6,p7,p8
516 D1B3 00          DB      0000_0000b  ;1G(p1/R17)-> VFD_P1_P8
517 D1B4 00          DB      0000_0000b  ;2G(p2/R16)
518 D1B5 00          DB      0000_0000b  ;3G(p3/R15)
519 D1B6 00          DB      0000_0000b  ;4G(p4/R14)
520 D1B7 00          DB      0000_0000b  ;5G(p5/R13)
521 D1B8 00          DB      0000_0000b  ;6G(p6/R12)
522 D1B9 00          DB      0000_0000b  ;7G(p7/R11)
523 D1BA 00          DB      0000_0000b  ;8G(p8/R10)
524                ;p9,p10,p11,p12_p13,p14,p15,p16
525 D1BB 00          DB      0000_0000b  ;1G(p9/R07)->VFD_P9_P16
526 D1BC 00          DB      0000_0000b  ;2G(p10/R06)
527 D1BD 00          DB      0000_0000b  ;3G(p11/R05)
528 D1BE 00          DB      0000_0000b  ;4G(p12/R04)
529 D1BF 00          DB      0000_0000b  ;5G(p13/R03)
530 D1C0 00          DB      0000_0000b  ;6G(p14/R02)
531 D1C1 00          DB      0000_0000b  ;7G(p15/R01)
532 D1C2 00          DB      0000_0000b  ;8G(p16/R00)
533
534                END

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-- 0 Error(s) --

--- Total Machine Code : 455 Bytes ---

**NOTE:**