CodeGen32 Revision history

Version	Date	Description
V1.019.22	2026/10/01	Modifications related to A31M22x: Fixed adc_buf error
V1.019.21	2026/08/27	Modifications related to A31M22x: scu.c, AF settings, Default settings (XIN, XOUT, RXD0, TXD0), Debug Message output modified
V1.019.20	2026/08/11	Applying PLL clock (hclk, pclk) usage settings and fixing FLM file link errors on A31M22x
V1.019.19	2026/06/26	Modified the setting PLL Clock(hclk, pclk) value in A31M22x.
V1.019.18	2026/05/29	Modified the setting UART Clock(Sel, div) value in A31M22x.
V1.019.17	2026/05/21	Modified the setting PLL(PLLCLKSEL) value in A31M22x.
V1.019.17+rc.P1	2025/10/29	Modified the setting ADC(EOCIE, EOSIE) value in A31M22x.
V1.019.16	2025/10/17	Apply accumulated changes and deploy horizontally.
V1.019.16+rc.P4	2025/09/25	Modified Clock initial function in A31T21x.
V1.019.16+rc.P3	2025/09/24	Modified the setting Timer.PRS value in A31M22x.
V1.019.16+rc.P2	2025/09/12	Modified the setting value and offset of pull-up resistor in A31M22x.
V1.019.16+rc.P1	2025/09/10	Modified A31M22x ADC Function. (adc.c)
V1.019.15	2025/07/07	Added MPWM Control function. (MPWM_OLR_POCxx)
V1.019.14	2025/05/19	Default value change: A31M22x MCLK (HSI)

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V1.019.13	2025/04/30	Default value change: A31M22x MCLK Remove compile warning : A33G53x, A33G52x File Copy Error Improvement
V1.019.12	2025/04/01	Added A31G33x series.
V1.019.11	2025/03/11	Added A31M22x series.
V1.019.10	2025/01/10	The HSI clock mismatch has been corrected, and the PLL output clock frequency has been limited in the clock tree of the A34M456.
V1.019.09	2024/12/30	Added A34M45x series.
V1.019.08	2024/12/06	Added A34M42x series.
V1.019.07	2024/04/01	Added to create setting AFSR2 register value. (A31T214)
V1.019.06	2024/02/26	Added A33G53x series.
V1.019.05	2023/12/12	Corrected alternative function of PA4, PA5 pins for all A31L22x packages.
V1.019.04	2023/11/30	Fixed bugs where A31G12x and A31R71x WDT interrupt setting values were not applied. Added A31S13x Series.
V1.019.02	2023/08/02	Changed the 32LQFP package name from A31G11xKL to A31G11xKN. Corrected the SEG pin number of all A31G11x packages. Added the pin map of the A31G112KY (32QFN-0505) package
V1.019.02	2023/07/18	Unsupported pins in the package are set to the ‘reserved’ or ‘analog input’. - A31G31x, A31G21x, A31G22x, A31G32x, A31G11x, A31G12x, A31L12x, A31L21x, A31L22x, A31R71x, A31T21x
V1.019.01	2023/6/19	A31L123KNN pin 30 mismatch error fixed

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V1.019.00	2023/6/1	Cleanup of warnings and garbage codes in source code A31G22x port mismatch error fixed. A33G52x GPIO interrupt typo error fixed.
V1.018.21	2023/5/25	Latest version check feature has been implemented. A33G52x IAR default profile is set to Debug.
V1.018.19	2023/4/5	Timer T0C pin warning fixed - A33G52x, A33M11x, A34M418, A3C30M1x64: A33G52x input frequency display mismatch fixed. A33G52x timer routine modified. - Initialization sequence reinforced. - Timer interrupt routine added. SystemInit call for WDT reset included - A31G31x, A31G32x, A33G52x, AC30M1x64 A31G22x I2C SCL/SCH clock error display fixed.
V1.018.14	2023/2/17	Added A31L21x series. Added A31L22x series. A31L123KLz pins 6~10 naming error fixed A31T21x PLL input frequency bug fixed.
V1.018.11	2022/11/4	Clock MUX mismatch corrected in clock tree. - A31G11x/A31G12x, A31L12x, A31R71x A31L12x, A31R71x series device selection has been corrected.
V1.018.10	2022/9/23	A31G22x DAC_DR write value bug was fixed. DAC_BR register setting was removed.
B1.018.09	2022/9/21	All Timers Prescaler inputs should be Prescale value + 1. A31G22x TIMER1n ExtClock value bug was fixed.
B1.018.08	2022/9/20	A31G22x DAC.c library modified - A31G22x DAC_BUF_EN bit was applied - DACOUT1 -> DACOUT0 changed, DAC0~3 were removed.

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		A33G52x PMU.c library modified - A33G52x PMU.c type miscasting bug was fixed **CLKCmd(uint8_t) -> (uint32_t)
B1.018.07	2022/9/19	A31G21x/22x/31x MCCR Clock source bugs were fixed
B1.018.06	2022/9/16	A33M116 Timer GRA/GRB register was fixed as Duty and Period. A33M116 TRIGMOD, TRIGPNT registers were applied A34M418 period calcutation error was fixed. A31G213 SPI2x were added A31G2xx series SPI baudrate bug was fixed ADC11 typo in DMA option was corrected
B1.018.05	2022/9/5	UART Baudrate generation value was fixed. A33M116 ADC Init generation error was fixed. A33M116 External Clock comment was added A33G52x SystenClock.c PCCR and RESET Debounce was added
B1.018.04	2022/8/30	A33G52x interrupt handler function name was fixed. A33M116 LSI clock value was fixed from 1MHz to 500kHz. A33M116 Shut-down problem caused by ADC Select Timer Trigger was fixed. A33M116 64-LQFP SWCLK/SWDIO pin duplicated problem was fixed A33G527/A31G226 UART buffer size zero error in IAR Compiler was fixed.
B1.018.03	2022/8/30	“I2C Clock frequency too low” warning was fixed. I2C Speed setting line was added. XIN/XOUT not used warning was fixed.
B1.018.02	2022/7/29	GCC startup code was fixed A31L123 LCD source generation was added.
B1.018.01	2022/6/30	A31G32x USB VCP Echo example code added.

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B1.018.00	2022/6/17	A33M116 New library version A34M418 clock configurator bug was fixed.
V1.017.28	2022/4/29	Additional I2C->CR initialization has been fixed (ORing). Device numbers in the interrupt functions has been fixed.
V1.017.26	2022/2/17	GPIO Pin initialization bug has been fixed (PD1 and PD10 error) A31G32x with general peripheral has been implemented.
V1.017.25	2022/1/12	Eclipse project file generation for test.
V1.017.23	2022/1/11	Demonstration codes have been included DEBUG_MSG, USART_ECHO, UART_ECHO, LED_BLINKY

List of supported devices

Core Type	Devices				
Cortex-M4F	A34M418 A34M416 A34M414	A34M420	A34M456		
Cortex-M3	A33M116 A33M114	A33G527 A33G526 A33G524	A33G53x		
Cortex-M0+	A31G123 A31G122 A31G112 A31G111	A31G226 A31G224 A31G213 A31G212	A31G316 A31G314 A31G313 A31G324 A31G323 A31G336	A31L123 A31L122	A31S134
	A31T216 A31T214	A31R713 A31R712	A31M223	A31L213 A31L214 A31L221 A31L222	
Cortex-M0	AC30M1464 AC30M1364				
Cortex-M3	AC33M8128 AC33M6128	AC33M4064 AC33M3064			